Příloha číslo 1

Katalogový list: Integrovaný budič IGBT a MOSFET tranzistorů IR2110

International
IOR Rectifier

IR2110(S)/IR2113(S) & (PbF)

HIGH AND LOW SIDE DRIVER

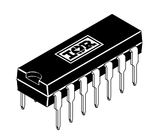
Features

- Floating channel designed for bootstrap operation
  Fully operational to +500V or +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
  Separate logic supply range from 3.3V to 20V
  Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Also available LEAD-FREE

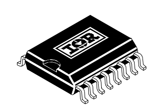
Product Summary

V_{OFFSET}	(IR2110)	500V max.
	(IR2113)	600V max.
I_O+/-		2A / 2A
V_{OUT}		10 - 20V
$t_{on/off}$ (typ.)		120 & 94 ns
Delay Matching	(IR2110)	10 ns max.
	(IR2113)	20ns max.

Packages



14-Lead PDIP
IR2110/IR2113

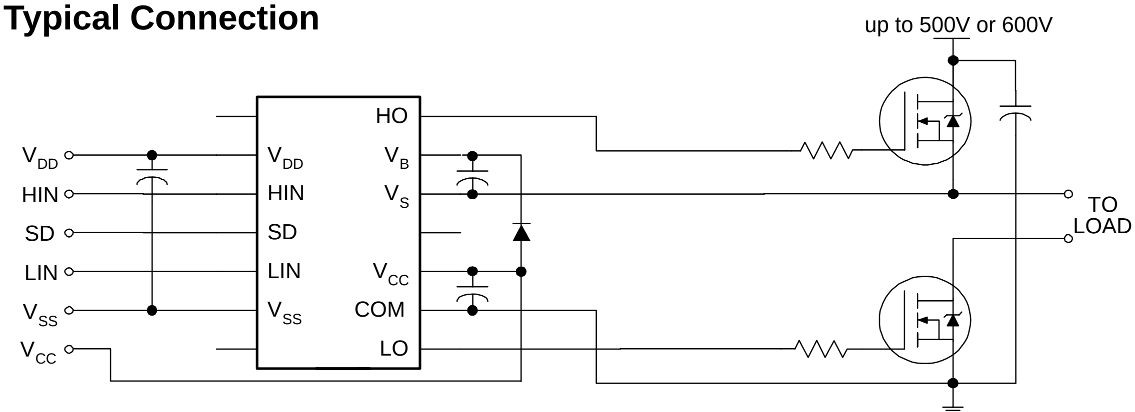


16-Lead SOIC
IR2110S/IR2113S

Description

The IR2110/IR2113 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 or 600 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage	(IR2110)	-0.3	525	V
		(IR2113)	-0.3	625	
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{DD}	Logic supply voltage		-0.3	V_{SS} + 25	
V_{SS}	Logic supply offset voltage		V_{CC} - 25	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN, LIN & SD)		V_{SS} - 0.3	V_{DD} + 0.3	
dV_s/dt	Allowable offset supply voltage transient (figure 2)		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq$ +25°C	(14 lead DIP)	—	1.6	W
		(16 lead SOIC)	—	1.25	
R_{THJA}	Thermal resistance, junction to ambient	(14 lead DIP)	—	75	°C/W
		(16 lead SOIC)	—	100	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in figures 36 and 37.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply absolute voltage		V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	(IR2110)	Note 1	500	
		(IR2113)	Note 1	600	
V_{HO}	High side floating output voltage		V_S	V_B	
V_{CC}	Low side fixed supply voltage		10	20	
V_{LO}	Low side output voltage		0	VCC	
V_{DD}	Logic supply voltage		V_{SS} + 3	V_{SS} + 20	
V_{SS}	Logic supply offset voltage		-5 (Note 2)	5	
V_{IN}	Logic input voltage (HIN, LIN & SD)		V_{SS}	V_{DD}	
T_A	Ambient temperature		-40	125	°C

Note 1: Logic operational for V_S of -4 to +500V. Logic state held for V_S of -4V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).
Note 2: When V_{DD} < 5V, the minimum V_{SS} offset is limited to $-V_{DD}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

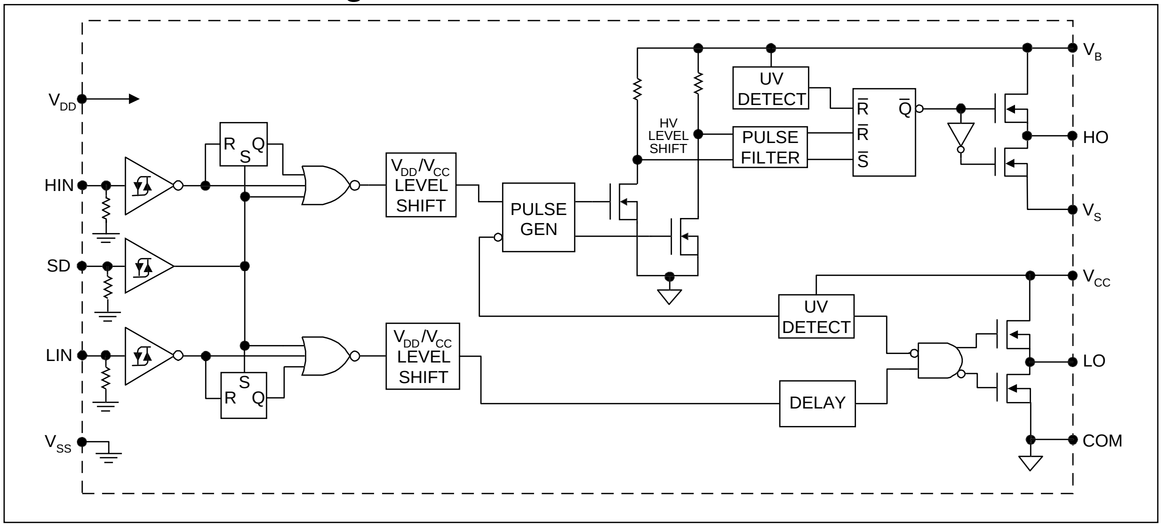
Symbol	Definition		Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay		7	—	120	150	ns	V_S = 0V
t_{off}	Turn-off propagation delay		8	—	94	125		V_S = 500V/600V
t_{sd}	Shutdown propagation delay		9	—	110	140		V_S = 500V/600V
t_r	Turn-on rise time		10	—	25	35		
t_f	Turn-off fall time		11	—	17	25		
MT	Delay matching, HS & LS	(IR2110)	—	—	—	10		
	turn-on/off	(IR2113)	—	—	—	20		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” input voltage	12	9.5	—	—	V	
V_{IL}	Logic “0” input voltage	13	—	—	6.0		
V_{OH}	High level output voltage, V_{BIAS} - V_O	14	—	—	1.2		I_O = 0A
V_{OL}	Low level output voltage, V_O	15	—	—	0.1		I_O = 0A
I_{LK}	Offset supply leakage current	16	—	—	50	µA	V_B=V_S = 500V/600V
I_{QBS}	Quiescent V_{BS} supply current	17	—	125	230		V_{IN} = 0V or V_{DD}
I_{QCC}	Quiescent V_{CC} supply current	18	—	180	340		V_{IN} = 0V or V_{DD}
I_{QDD}	Quiescent V_{DD} supply current	19	—	15	30		V_{IN} = 0V or V_{DD}
I_{IN+}	Logic “1” input bias current	20	—	20	40		V_{IN} = V_{DD}
I_{IN-}	Logic “0” input bias current	21	—	—	1.0		V_{IN} = 0V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	22	7.5	8.6	9.7	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	23	7.0	8.2	9.4		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	24	7.4	8.5	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	25	7.0	8.2	9.4		
I_{O+}	Output high short circuit pulsed current	26	2.0	2.5	—	A	V_O = 0V, V_{IN} = V_{DD} PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	27	2.0	2.5	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

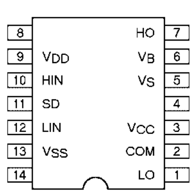
Functional Block Diagram



Lead Definitions

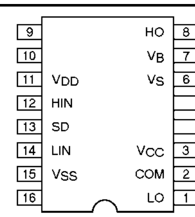
Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



14 Lead PDIP

IR2110/IR2113



16 Lead SOIC (Wide Body)

IR2110S/IR2113S

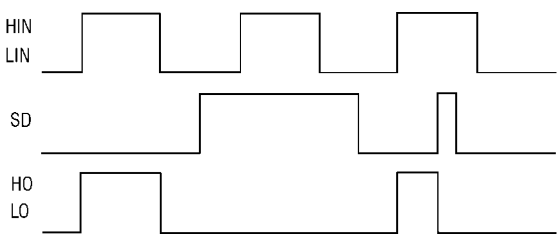


Figure 1. Input/Output Timing Diagram

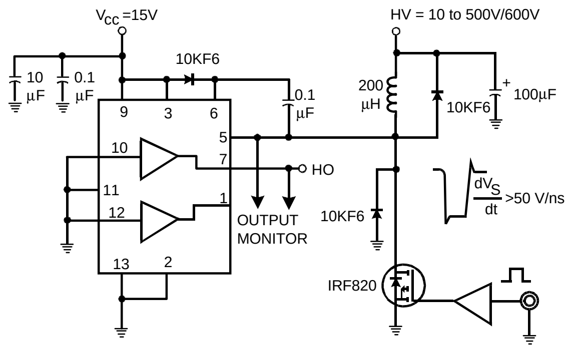


Figure 2. Floating Supply Voltage Transient Test Circuit

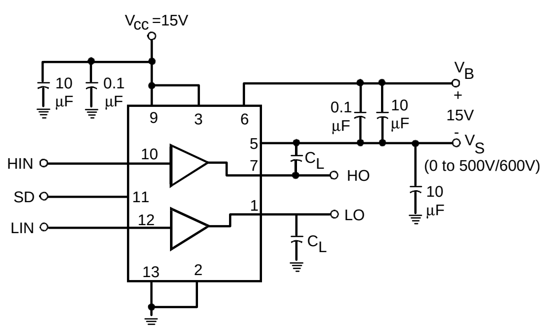


Figure 3. Switching Time Test Circuit

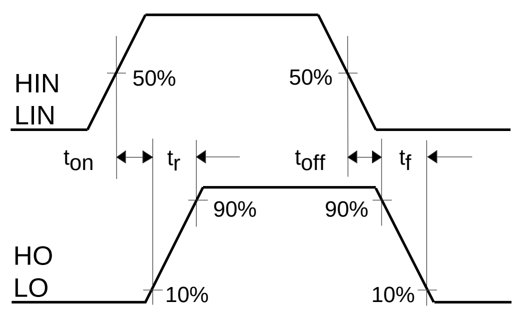


Figure 4. Switching Time Waveform Definition

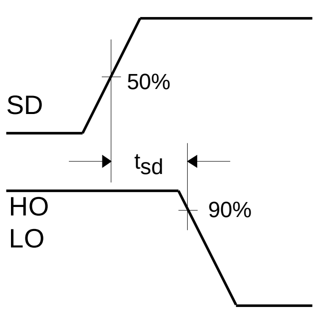


Figure 5. Shutdown Waveform Definitions

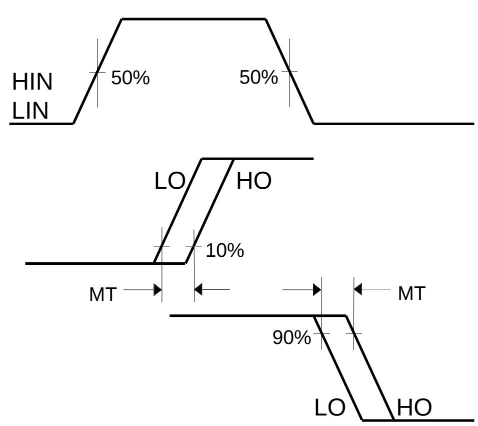


Figure 6. Delay Matching Waveform Definitions

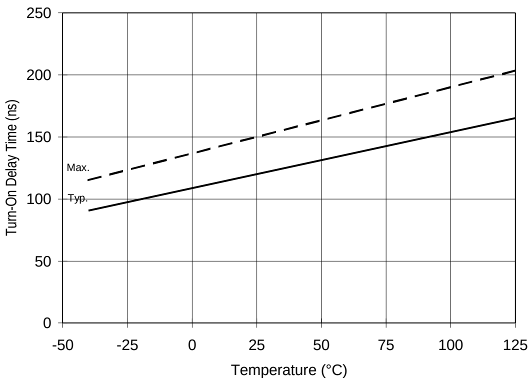


Figure 7A. Turn-On Time vs. Temperature

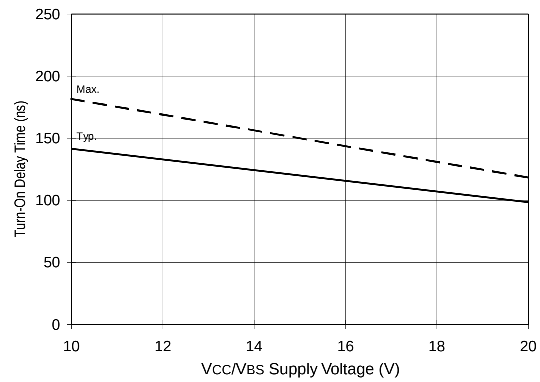


Figure 7B. Turn-On Time vs. VCC/VBS Supply Voltage

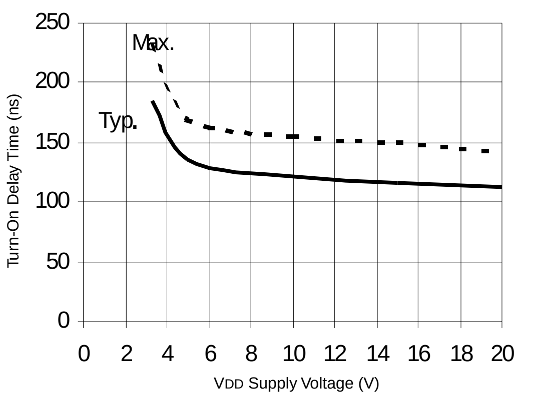


Figure 7C. Turn-On Time vs. VDD Supply Voltage

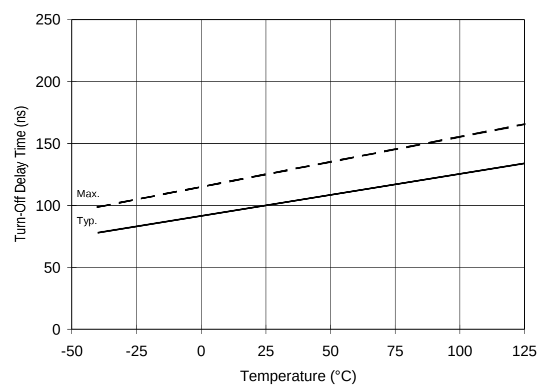


Figure 8A. Turn-Off Time vs. Temperature

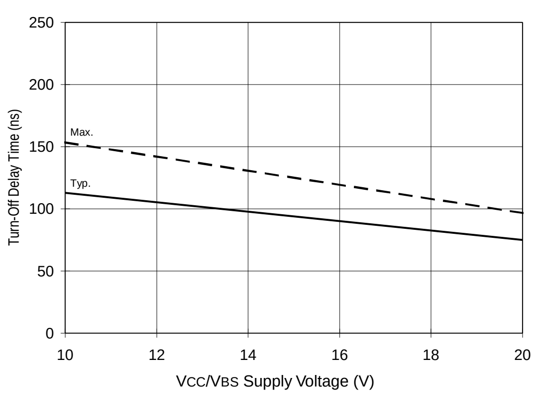


Figure 8B. Turn-Off Time vs. VCC/VBS Supply Voltage

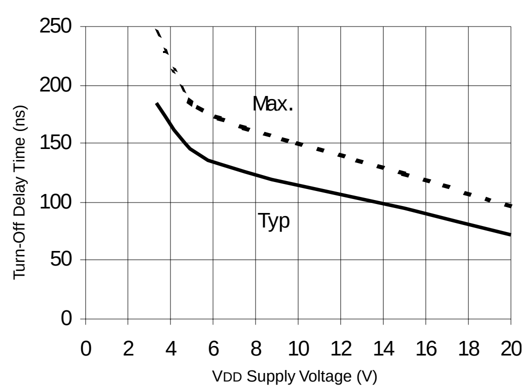


Figure 8C. Turn-Off Time vs. VDD Supply Voltage

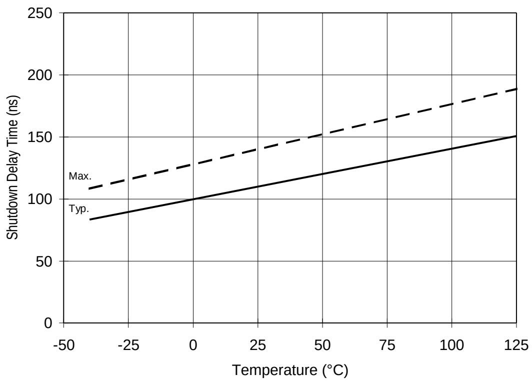


Figure 9A. Shutdown Time vs. Temperature

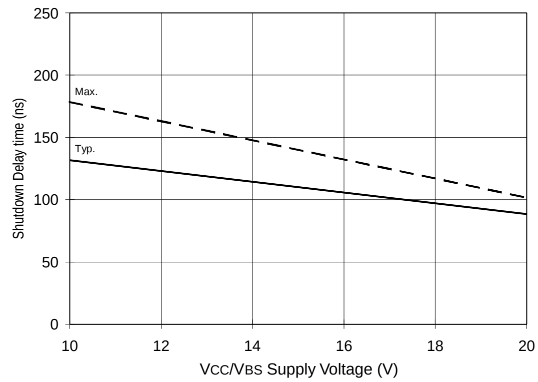


Figure 9B. Shutdown Time vs. VCC/VBS Supply Voltage

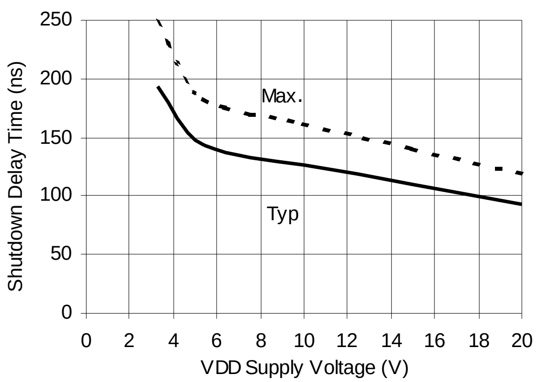


Figure 9C. Shutdown Time vs. VDD Supply Voltage

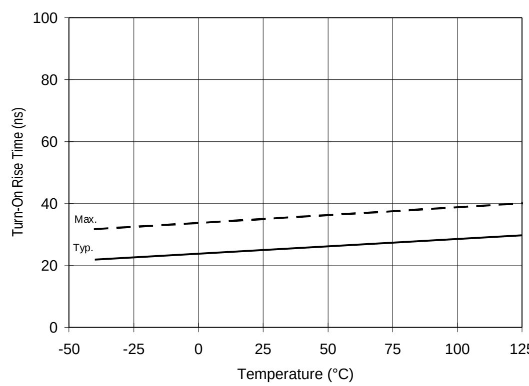


Figure 10A. Turn-On Rise Time vs. Temperature

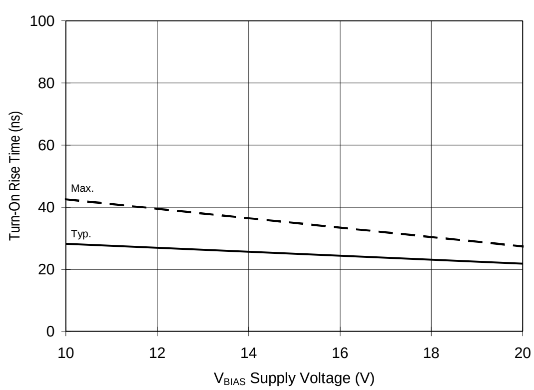


Figure 10B. Turn-On Rise Time vs. Voltage

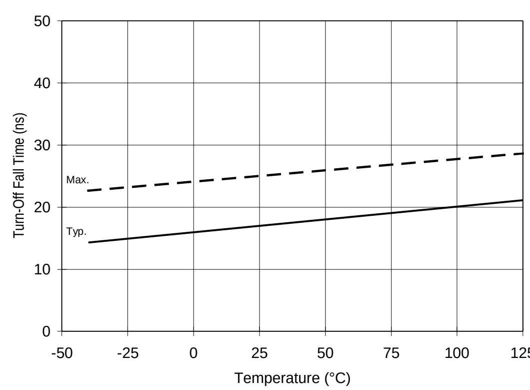


Figure 11A. Turn-Off Fall Time vs. Temperature

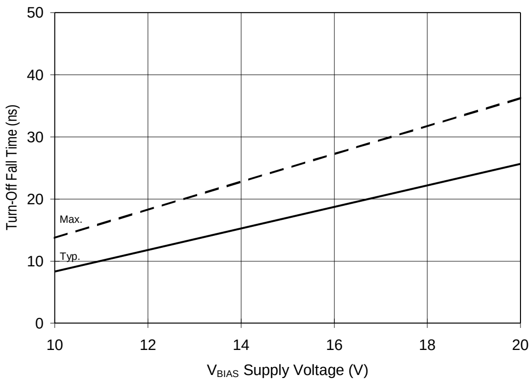


Figure 11B. Turn-Off Fall Time vs. Voltage

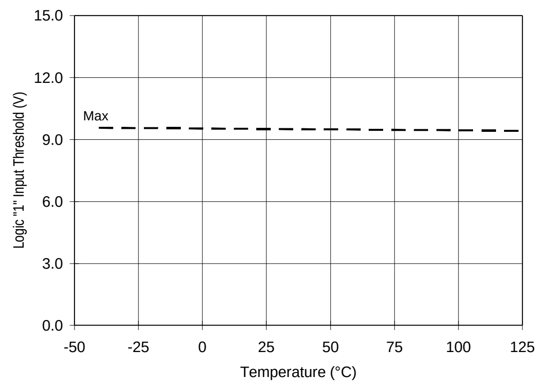


Figure 12A. Logic “1” Input Threshold vs. Temperature

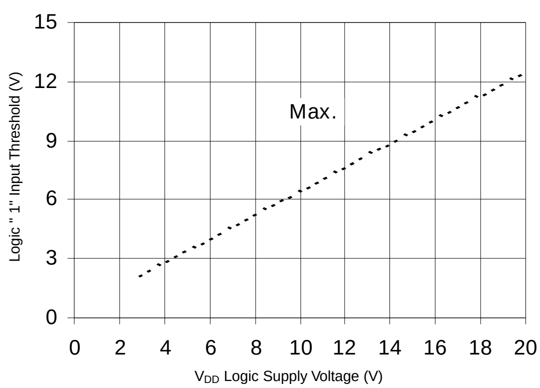


Figure 12B. Logic “1” Input Threshold vs. Voltage

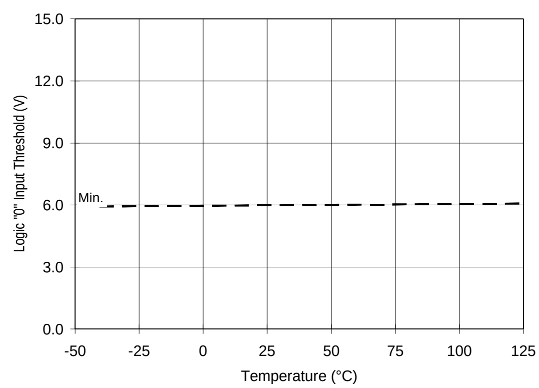


Figure 13A. Logic “0” Input Threshold vs. Temperature

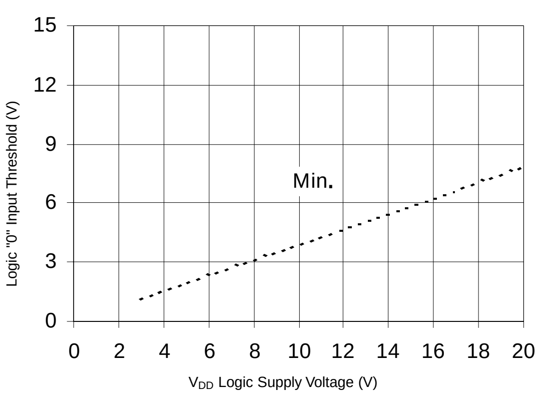


Figure 13B. Logic “0” Input Threshold vs. Voltage

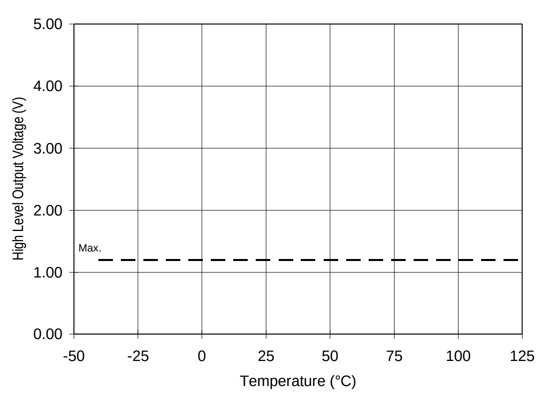


Figure 14A. High Level Output vs. Temperature

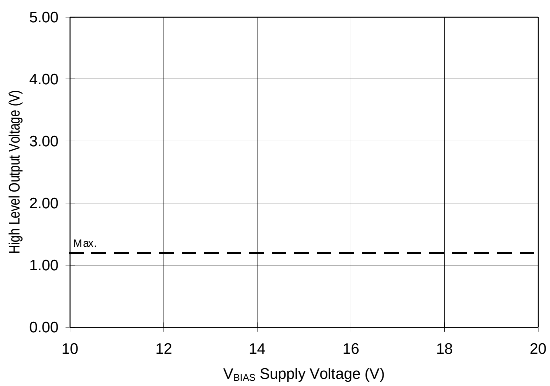


Figure 14B. High Level Output vs. Voltage

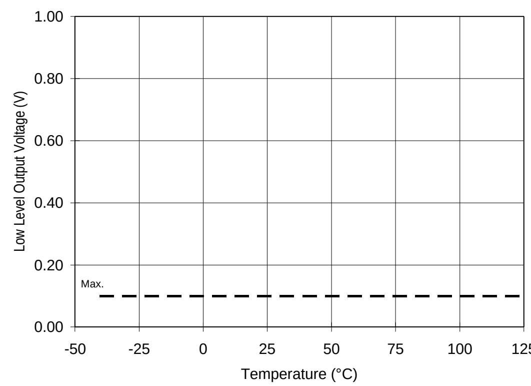


Figure 15A. Low Level Output vs. Temperature

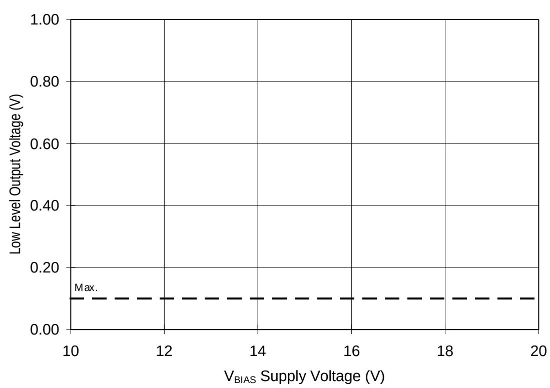


Figure 15B. Low Level Output vs. Voltage

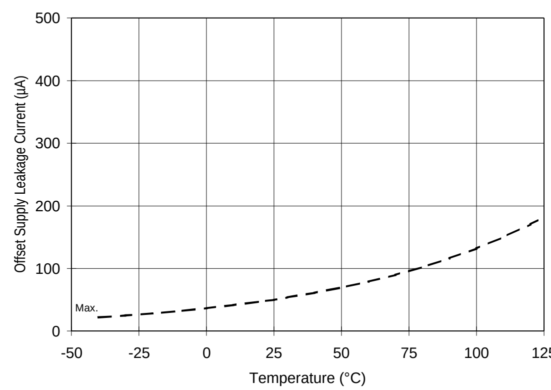


Figure 16A. Offset Supply Current vs. Temperature

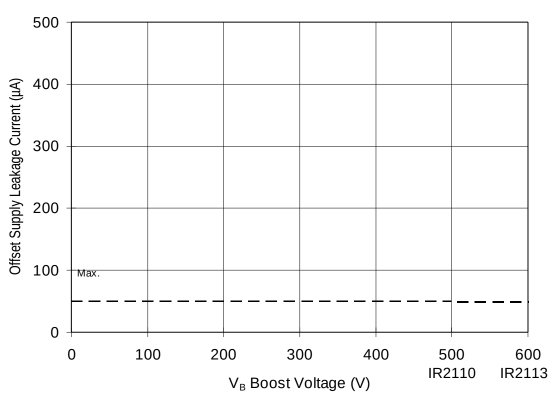


Figure 16B. Offset Supply Current vs. Voltage

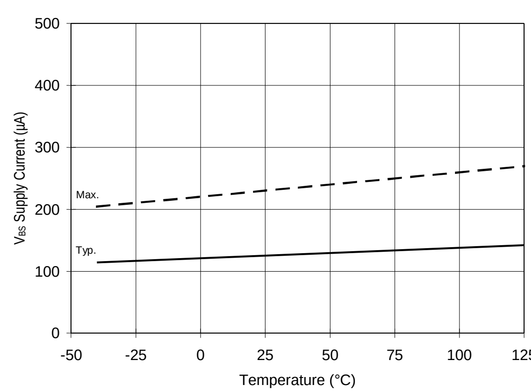


Figure 17A. V_{BS} Supply Current vs. Temperature

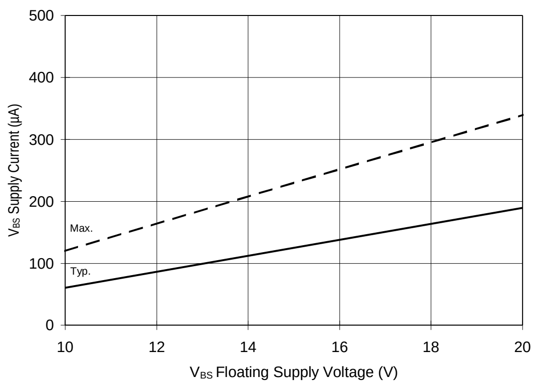


Figure 17B. V_{BS} Supply Current vs. Voltage

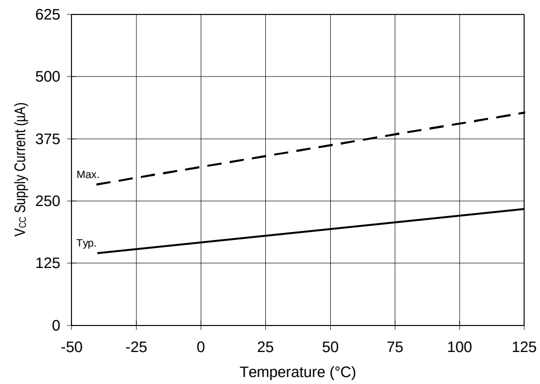


Figure 18A. V_{CC} Supply Current vs. Temperature

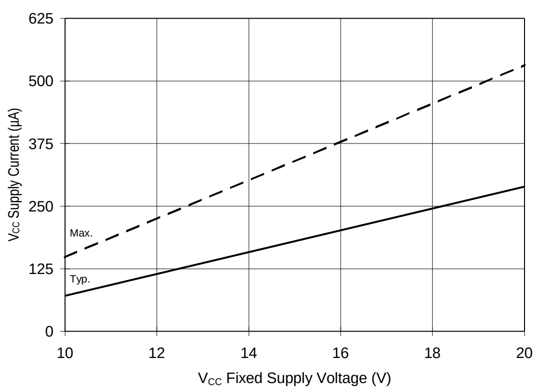


Figure 18B. V_{CC} Supply Current vs. Voltage

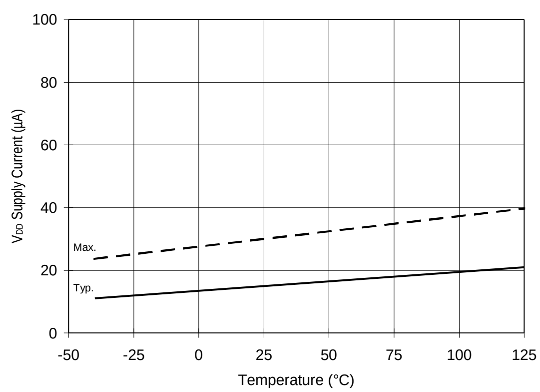


Figure 19A. V_{DD} Supply Current vs. Temperature

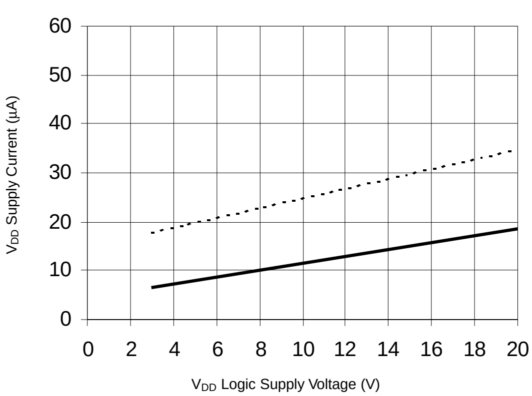


Figure 19B. V_{DD} Supply Current vs. V_{DD} Voltage

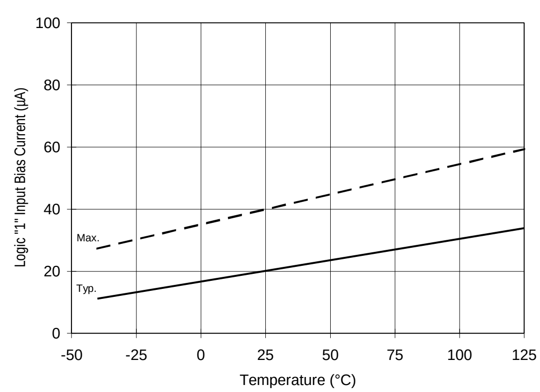


Figure 20A. Logic "1" Input Current vs. Temperature

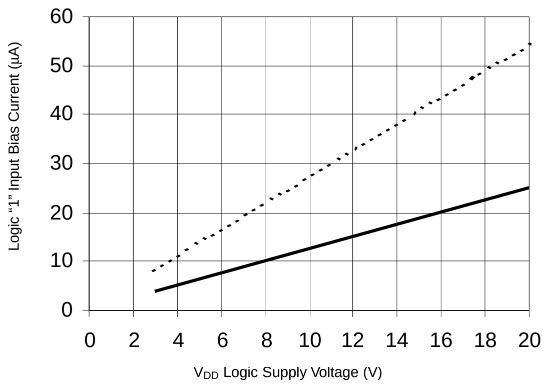


Figure 20B. Logic "1" Input Current vs. V_{DD} Voltage

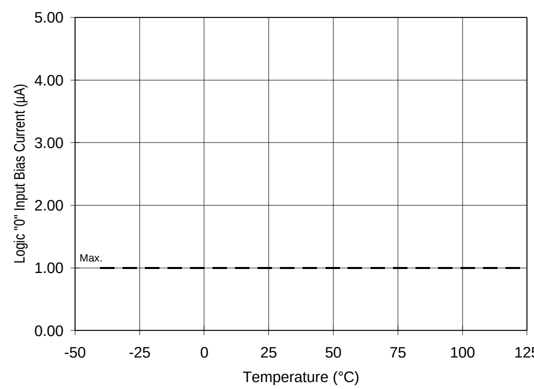


Figure 21A. Logic "0" Input Current vs. Temperature

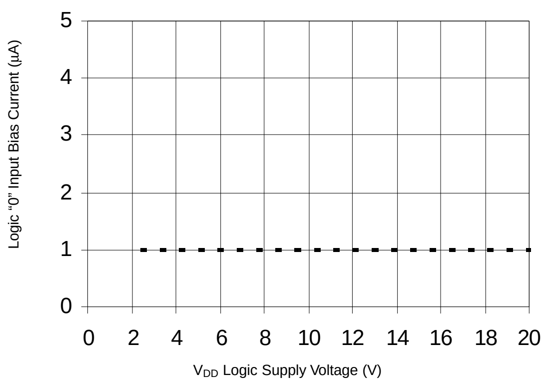


Figure 21B. Logic "0" Input Current vs. V_{DD} Voltage

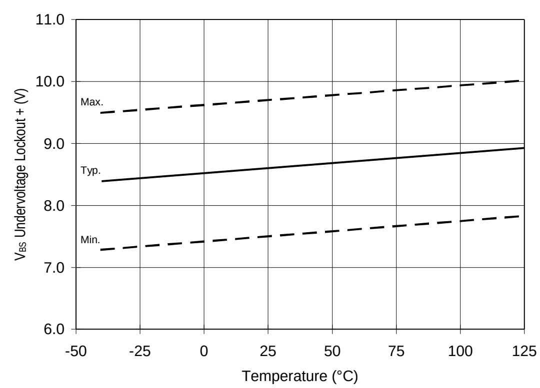


Figure 22. V_{BS} Undervoltage (+) vs. Temperature

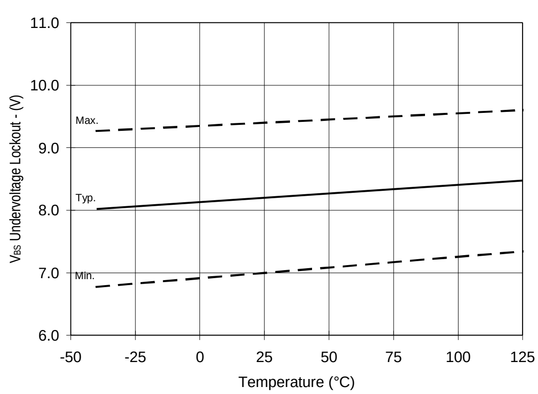


Figure 23. V_{BS} Undervoltage (-) vs. Temperature

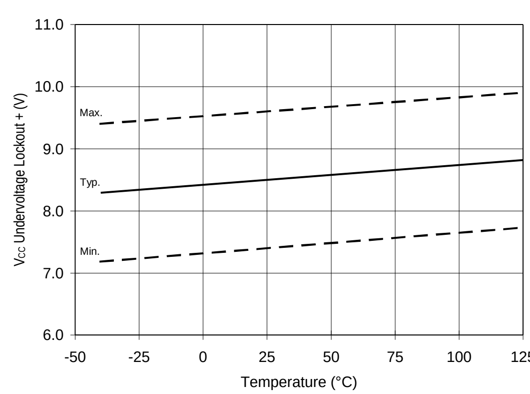


Figure 24. V_{CC} Undervoltage (+) vs. Temperature

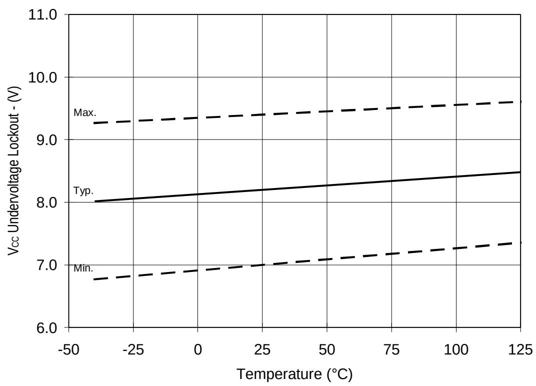


Figure 25. V_{CC} Undervoltage (-) vs. Temperature

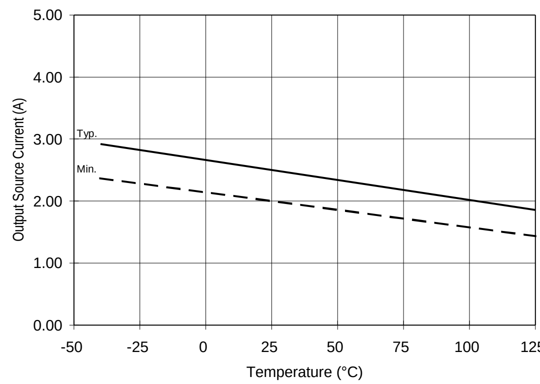


Figure 26A. Output Source Current vs. Temperature

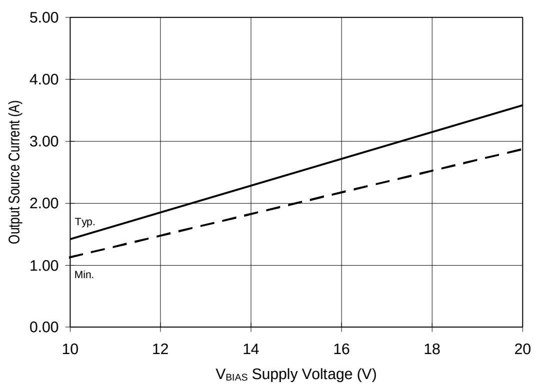


Figure 26B. Output Source Current vs. Voltage

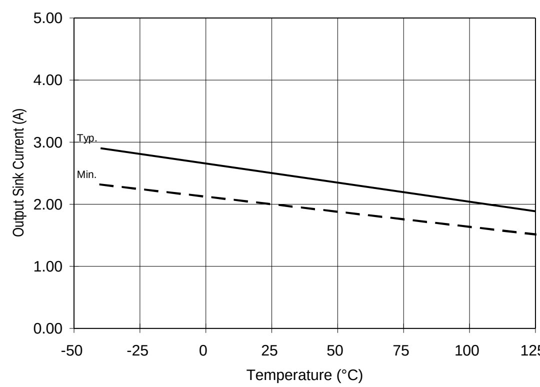


Figure 27A. Output Sink Current vs. Temperature

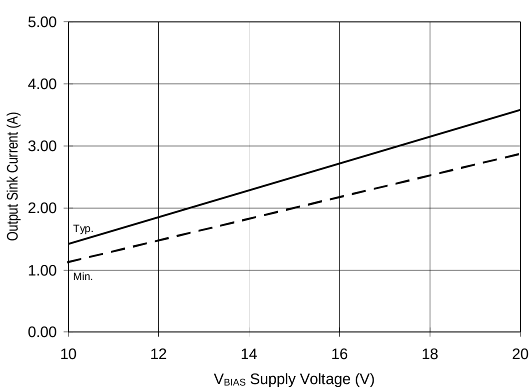


Figure 27B. Output Sink Current vs. Voltage

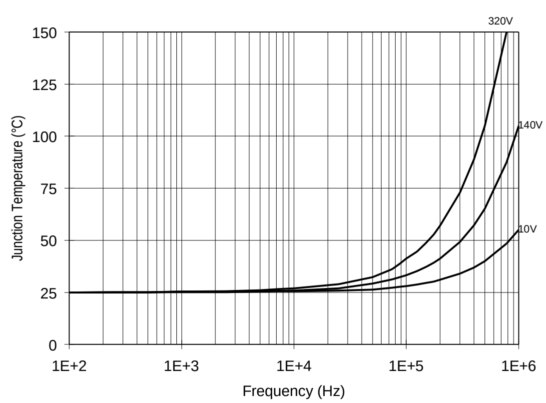


Figure 28. IR2110/IR2113 T_J vs. Frequency (IRFBC20) R_{GATE} = 33Ω, V_{CC} = 15V

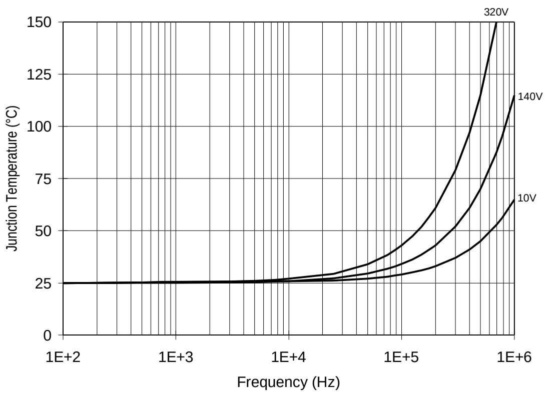


Figure 29. IR2110/IT2113 T_J vs. Frequency (IRFBC30) $R_{GATE} = 22\Omega$, $V_{CC} = 15V$

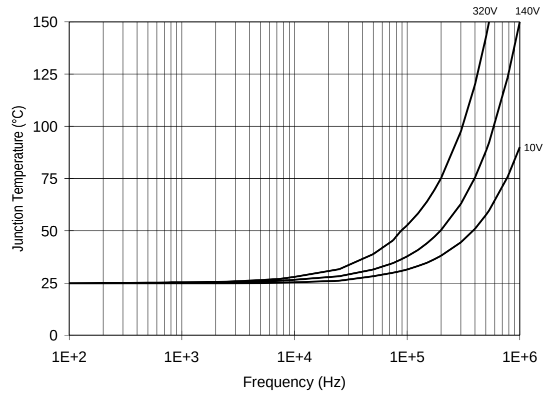


Figure 30. IR2110/IR2113 T_J vs. Frequency (IRFBC40) $R_{GATE} = 15\Omega$, $V_{CC} = 15V$

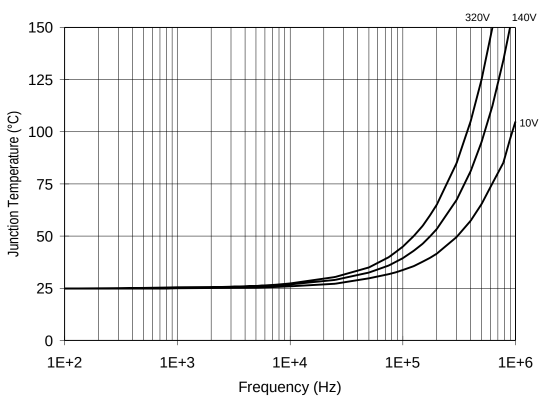


Figure 31. IR2110/IR2113 T_J vs. Frequency (IRFPE50) $R_{GATE} = 10\Omega$, $V_{CC} = 15V$

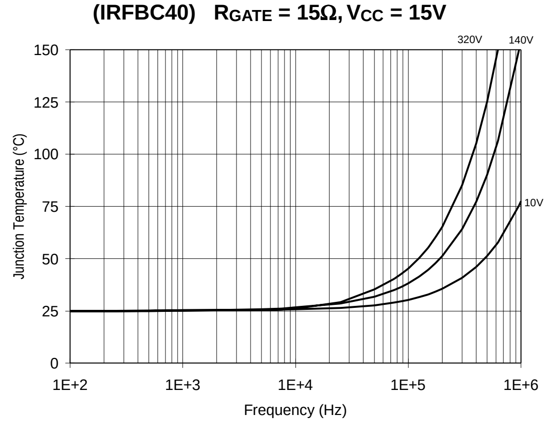


Figure 32. IR2110S/IR2113S T_J vs. Frequency (IRFBC20) $R_{GATE} = 33\Omega$, $V_{CC} = 15V$

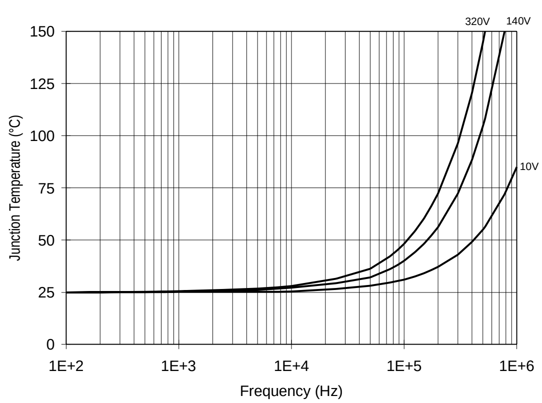


Figure 33. IR2110S/IR2113S T_J vs. Frequency (IRFBC30) $R_{GATE} = 22\Omega$, $V_{CC} = 15V$

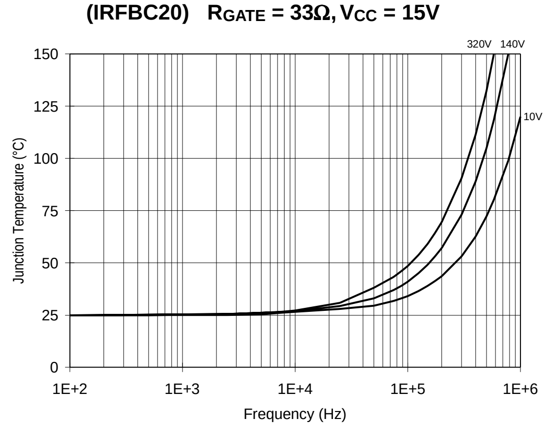


Figure 34. IR2110S/IR2113S T_J vs. Frequency (IRFBC40) $R_{GATE} = 15\Omega$, $V_{CC} = 15V$

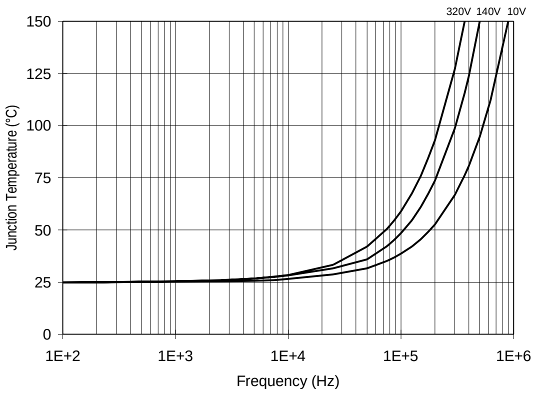


Figure 35. IR2110S/IR2113S T_J vs. Frequency (IRFPE50) R_{GATE} = 10Ω, V_{CC} = 15V

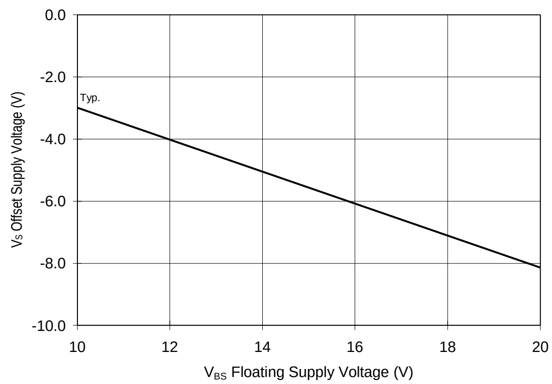


Figure 36. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

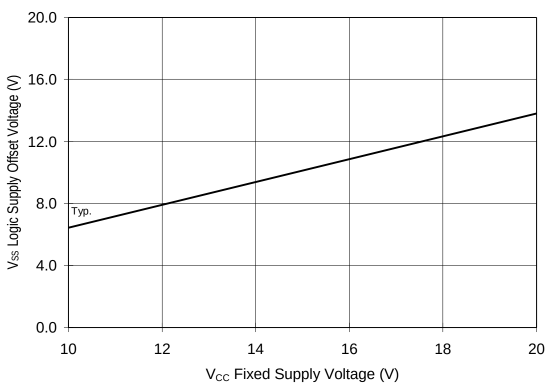
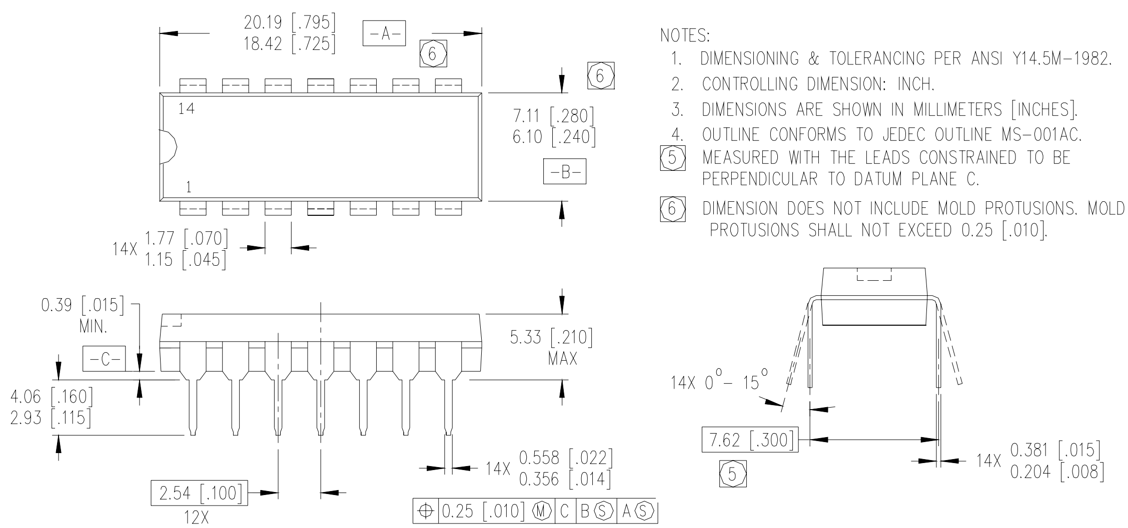


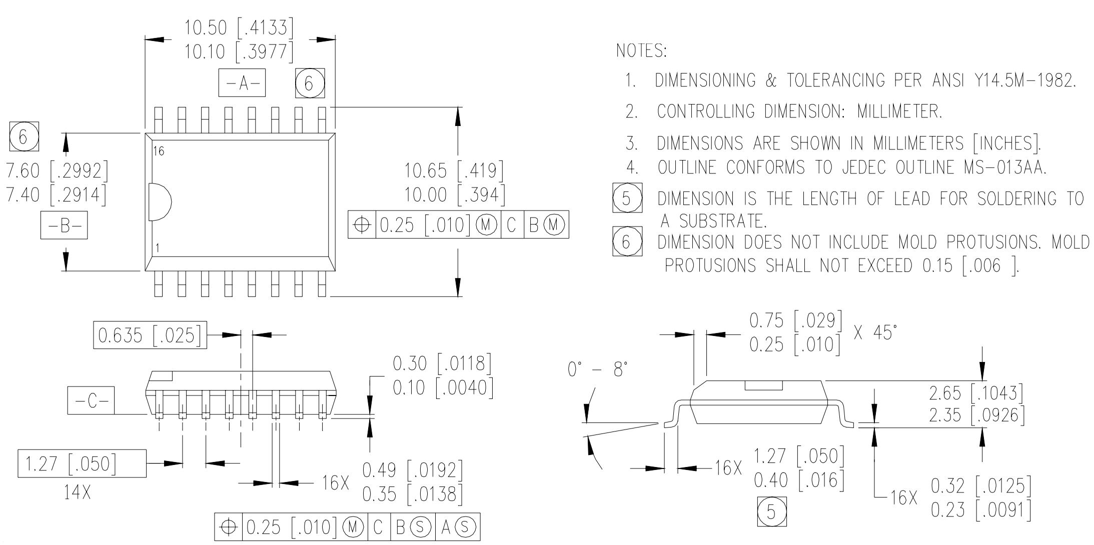
Figure 37. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage

Case Outlines



01-6010
01-3002 03 (MS-001AC)

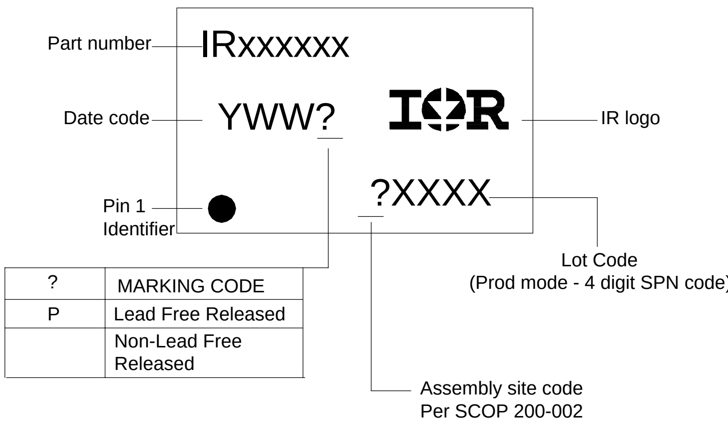
14-Lead PDIP



01 6015
01-3014 03 (MS-013AA)

16-Lead SOIC (wide body)

LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)
14-Lead IR2110 order IR2110
14-Lead IR2113 order IR2113
16-Lead IR2110S order IR2110S
16-Lead IR2113S order IR2113S

Leadfree Part
14-Lead IR2110 order IR2110PbF
14-Lead IR2113 order IR2113PbF
16-Lead IR2110S order IR2110SPbF
16-Lead IR2113S order IR2113SPbF

International Rectifier
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105

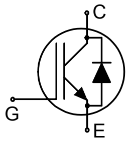
Příloha číslo 2

Katalogový list: Tranzistor IHW30N160R2

IHW30N160R2

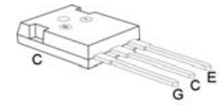
Soft Switching Series

TrenchStop® Reverse Conducting (RC-)IGBT with monolithic body diode



Features:

- Powerful monolithic Body Diode with very low forward voltage
- Body diode clamps negative voltages
- Trench and Fieldstop technology for 1600 V applications offers :
  - very tight parameter distribution
  - high ruggedness, temperature stable behavior
- NPT technology offers easy parallel switching capability due to positive temperature coefficient in $V_{CE(sat)}$
- Low EMI
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant
- Complete product spectrum and PSpice Models : http://www.infineon.com/igbt/



PG-TO-247-3

Applications:

- Inductive Cooking
- Soft Switching Applications

Type	V_{CE}	I_C	$V_{CE(sat),Tj=25°C}$	$T_{j,max}$	Marking	Package
IHW30N160R2	1600V	30A	1.8V	175°C	H30R1602	PG-TO-247-3

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CE}	1600	V
DC collector current T_C = 25°C T_C = 100°C	I_C	 60 30	A
Pulsed collector current, t_p limited by T_{jmax}	I_{Cpuls}	90	
Turn off safe operating area ($V_{CE} \leq$ 1600V, $T_j \leq$ 175°C)	-	90	
Diode forward current T_C = 25°C T_C = 100°C	I_F	 60 30	
Diode pulsed current, t_p limited by T_{jmax}	I_{Fpuls}	90	
Diode surge non repetitive current, t_p limited by T_{jmax} T_C = 25°C, t_p = 10ms, sine halfwave T_C = 25°C, $t_p \leq$ 2.5µs, sine halfwave T_C = 100°C, $t_p \leq$ 2.5µs, sine halfwave	I_{FSM}	 50 130 120	
Gate-emitter voltage Transient Gate-emitter voltage (t_p < 10 µs, D < 0.01)	V_{GE}	±20 ±25	V
Power dissipation T_C = 25°C	P_{tot}	312	W
Operating junction temperature	T_j	-40...+175	°C
Storage temperature	T_{stg}	-55...+175	
Soldering temperature, 1.6mm (0.063 in.) from case for 10s	-	260	

[1] J-STD-020 and JESD-022

Thermal Resistance

Parameter	Symbol	Conditions	Max. Value	Unit
Characteristic				
IGBT thermal resistance, junction – case	R_{thJC}		0.48	K/W
Diode thermal resistance, junction – case	R_{thJCD}		0.48	
Thermal resistance, junction – ambient	R_{thJA}		40	

Electrical Characteristic, at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value			Unit
			min.	Typ.	max.	
Static Characteristic						
Collector-emitter breakdown voltage	$V_{(BR)CES}$	V_{GE}=0V, I_C=500µA	1600	-	-	V
Collector-emitter saturation voltage	$V_{CE(sat)}$	V_{GE} = 15V, I_C=30A				
		T_j=25°C	-	1.8	2.1	
		T_j=150°C	-	2.25	-	
		T_j=175°C	-	2.35	-	
Diode forward voltage	V_F	V_{GE}=0V, I_F=30A				
		T_j=25°C	-	1.65	2.0	
		T_j=150°C	-	2.0	-	
		T_j=175°C	-	2.0	-	
Gate-emitter threshold voltage	$V_{GE(th)}$	I_C=0.75mA, V_{CE}=V_{GE}	5.1	5.8	6.4	
Zero gate voltage collector current	I_{CES}	V_{CE}=1600V, V_{GE}=0V				µA
		T_j=25°C	-	-	5	
		T_j=175°C	-	-	2500	
Gate-emitter leakage current	I_{GES}	V_{CE}=0V, V_{GE}=20V	-	-	100	nA
Transconductance	g_{fs}	V_{CE}=20V, I_C=30A	-	22.5	-	S
Integrated gate resistor	R_{Gint}			none		Ω

Dynamic Characteristic

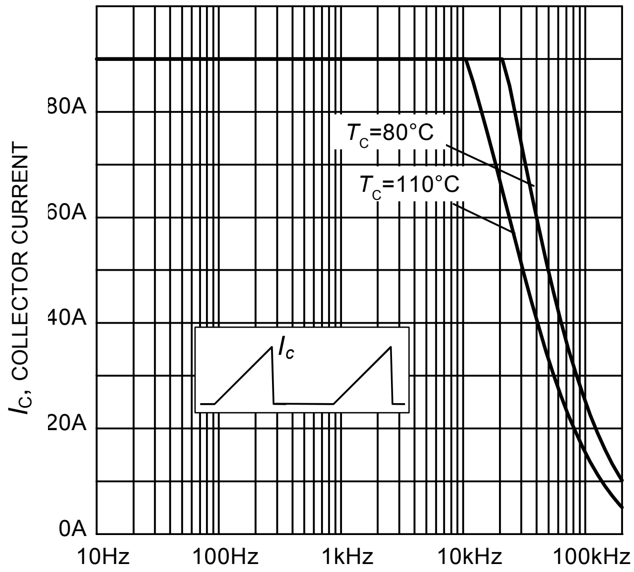
Input capacitance	C_{iss}	V_{CE}=25V, V_{GE}=0V, f=1MHz	-	2740	-	pF
Output capacitance	C_{oss}		-	68.1	-	
Reverse transfer capacitance	C_{rss}		-	58.7	-	
Gate charge	Q_{Gate}	V_{CC}=1280V, I_C=30A; V_{GE}=15V	-	94	-	nC
Internal emitter inductance measured 5mm (0.197 in.) from case	L_E		-	13	-	nH

Switching Characteristic, Inductive Load, at T_j=25 °C

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
IGBT Characteristic						
Turn-off delay time	$t_{d(off)}$	T_j=25°C, V_{CC}=600V, I_C=30A V_{GE}=0 /15V, R_G=10Ω	-	525	-	ns
Fall time	t_f		-	38.3	-	
Turn-on energy	E_{on}		-	-	-	
Turn-off energy	E_{off}		-	2.53	-	mJ
Total switching energy	E_{ts}		-	2.53	-	

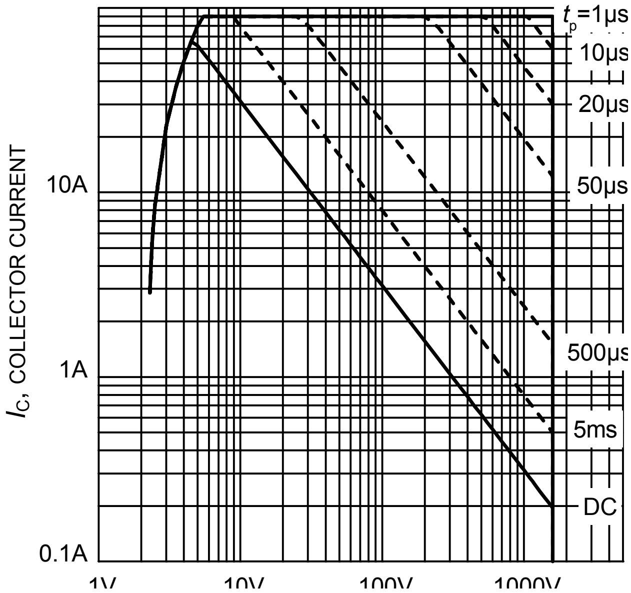
Switching Characteristic, Inductive Load, at T_j=175 °C

Parameter	Symbol	Conditions	Value			Unit
			min.	Typ.	max.	
IGBT Characteristic						
Turn-off delay time	$t_{d(off)}$	T_j=175°C V_{CC}=600V, I_C=30A, V_{GE}= 0 /15V, R_G= 10Ω	-	564	-	ns
Fall time	t_f		-	111	-	
Turn-on energy	E_{on}		-	-	-	
Turn-off energy	E_{off}		-	4.37	-	mJ
Total switching energy	E_{ts}		-	4.37	-	



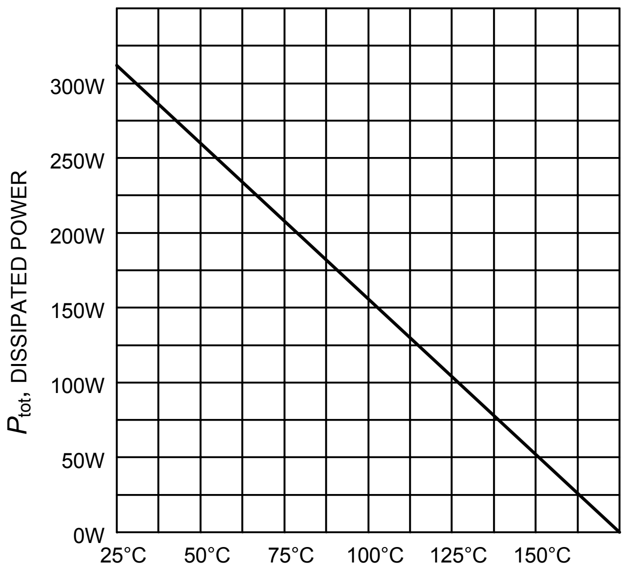
f, SWITCHING FREQUENCY

Figure 1. Collector current as a function of switching frequency for hard switching (turn-off)
($T_j \leq 175°C$, $D = 0.5$, $V_{CE} = 600V$, $V_{GE} = 0/+15V$, $R_G = 10\Omega$)



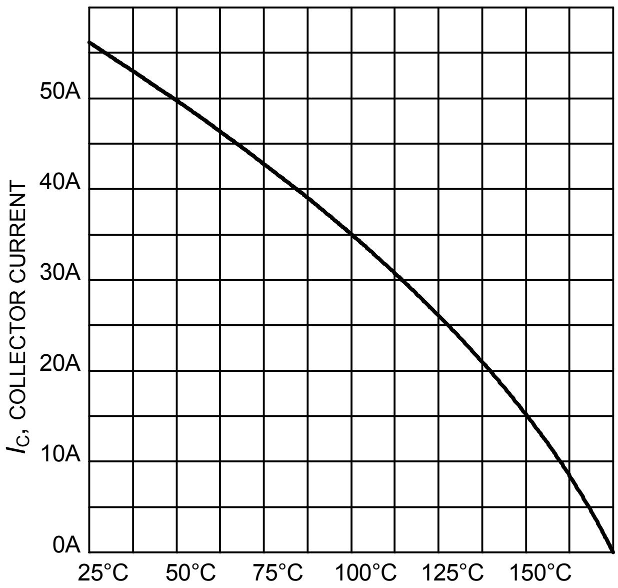
V_{CE}, COLLECTOR-EMITTER VOLTAGE

Figure 2. IGBT Safe operating area
($D = 0$, $T_C = 25°C$, $T_j \leq 175°C$; V_{GE}=15V)



T_C, CASE TEMPERATURE

Figure 3. Power dissipation as a function of case temperature
($T_j \leq 175°C$)



T_C, CASE TEMPERATURE

Figure 4. DC Collector current as a function of case temperature
($V_{GE} \geq 15V$, $T_j \leq 175°C$)

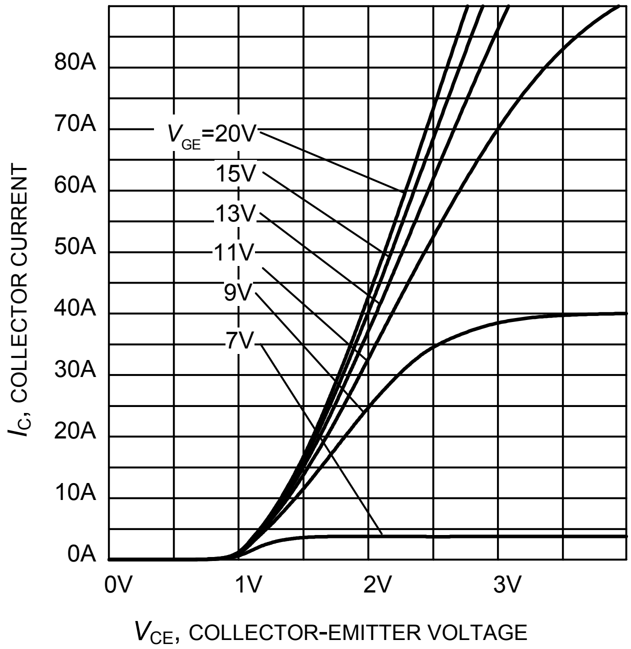


Figure 5. Typical output characteristic
(T_j = 25°C)

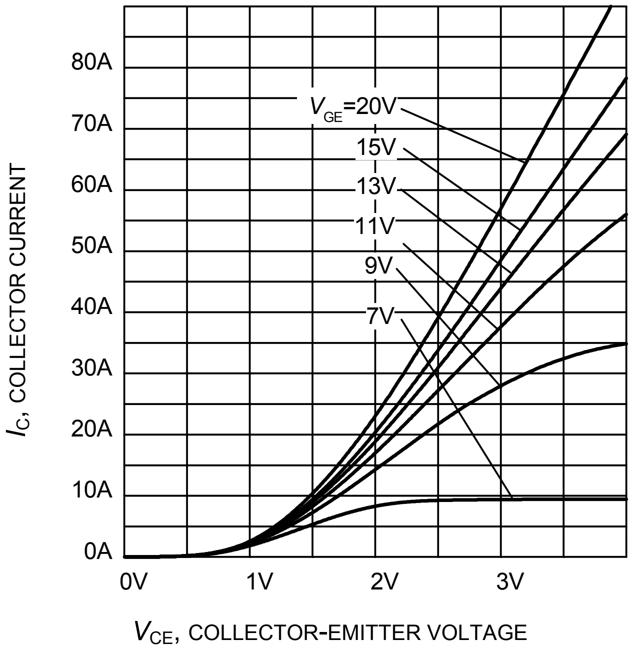


Figure 6. Typical output characteristic
(T_j = 175°C)

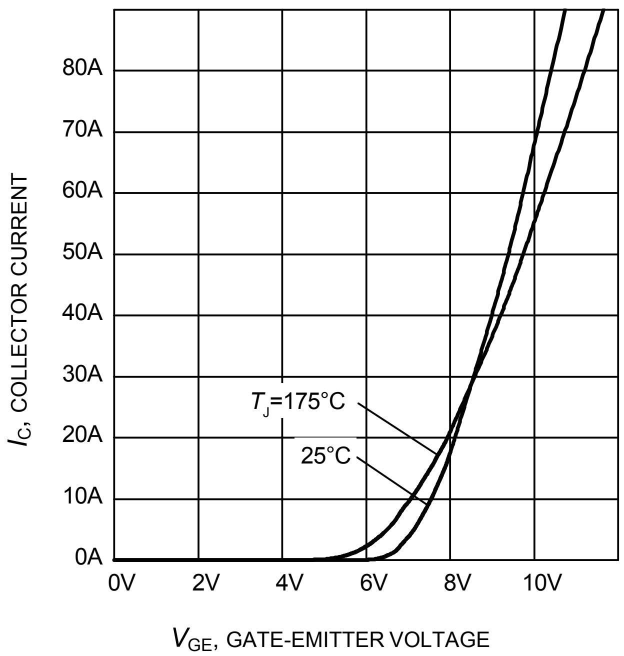


Figure 7. Typical transfer characteristic
(V_{CE}=20V)

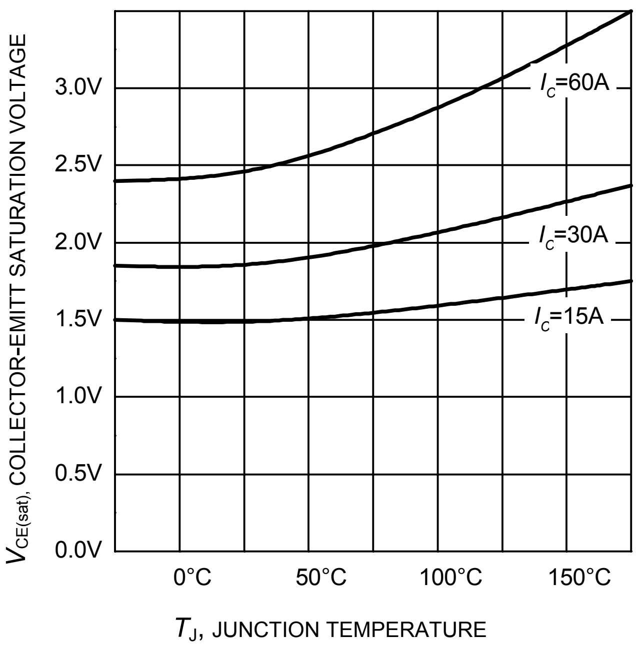


Figure 8. Typical collector-emitter saturation voltage as a function of junction temperature
(V_{GE} =15V)

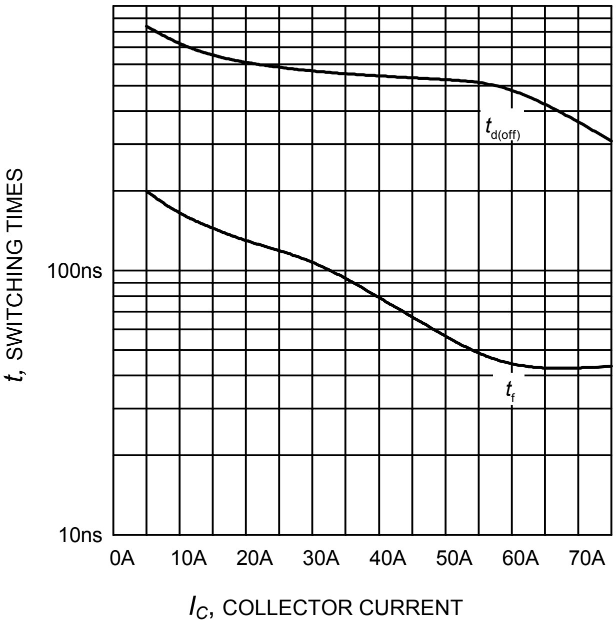


Figure 9. Typical switching times as a function of collector current
(inductive load, T_J=175°C, V_{CE}=600V, V_{GE}=0/15V, R_G=10Ω, Dynamic test circuit in Figure E)

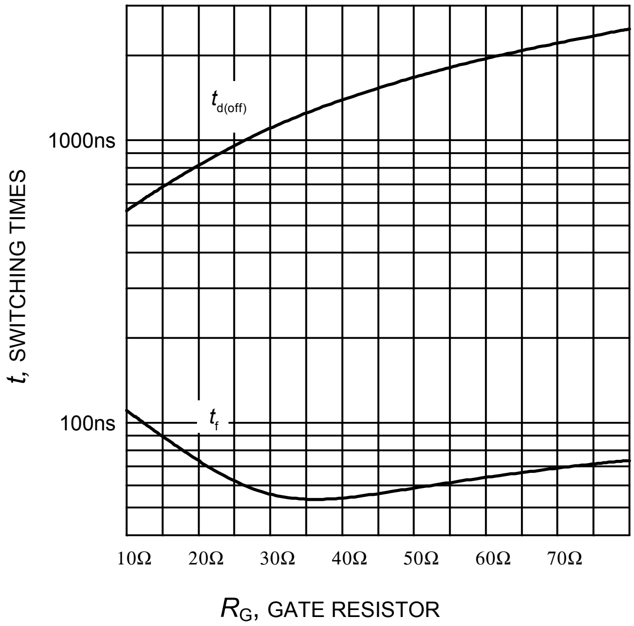


Figure 10. Typical switching times as a function of gate resistor
(inductive load, T_J=175°C, V_{CE}=600V, V_{GE}=0/15V, I_C=30A, Dynamic test circuit in Figure E)

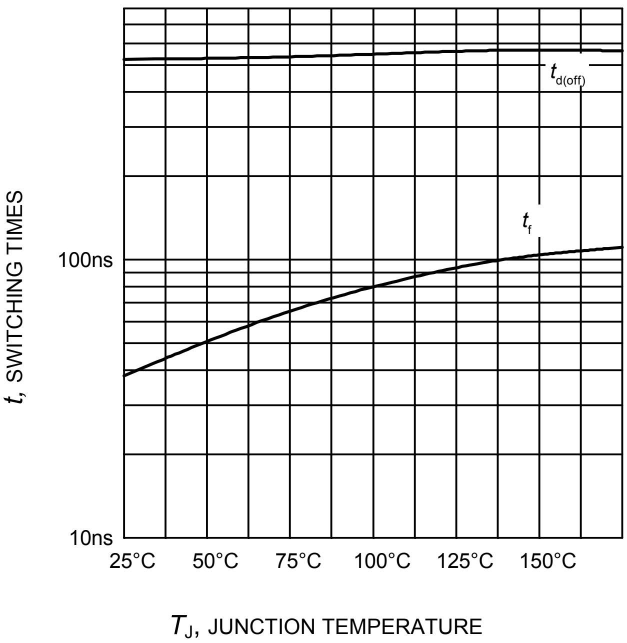


Figure 11. Typical switching times as a function of junction temperature
(inductive load, V_{CE}=600V, V_{GE}=0/15V, I_C=30A, R_G=10Ω, Dynamic test circuit in Figure E)

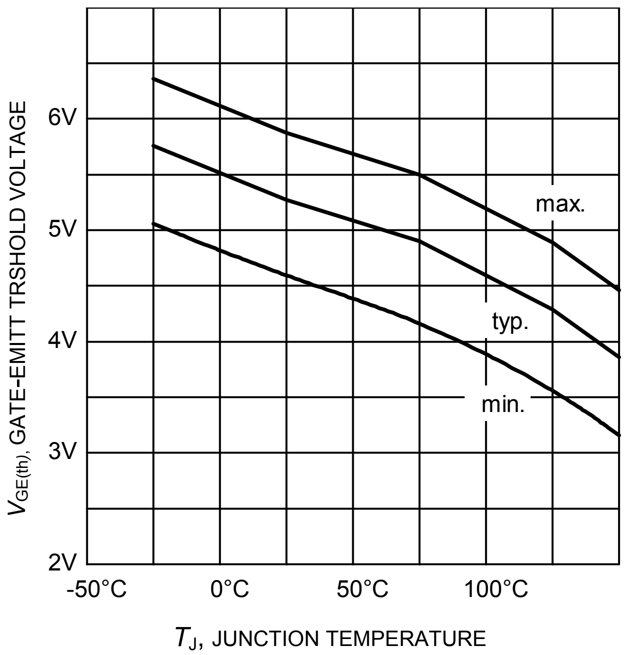
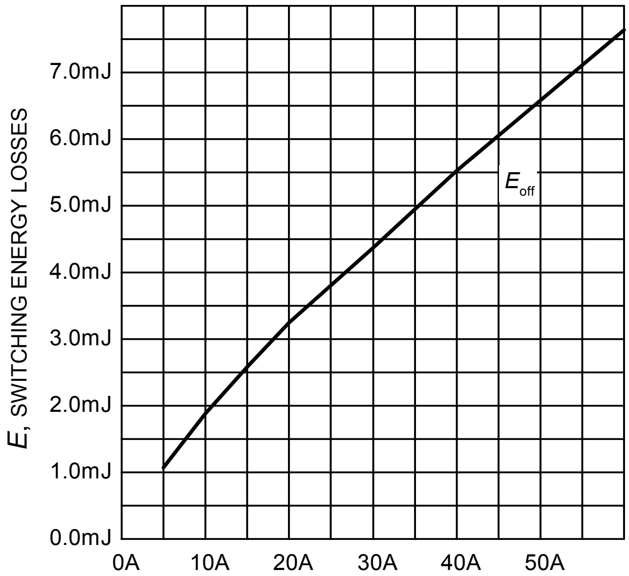
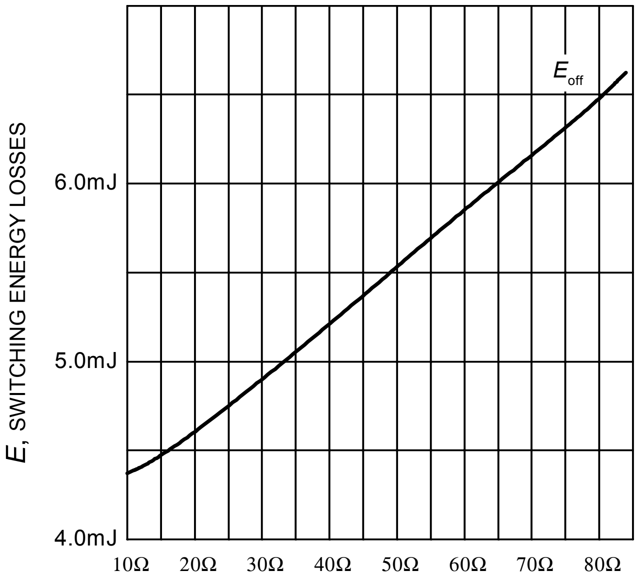


Figure 12. Gate-emitter threshold voltage as a function of junction temperature
(I_C = 0.15mA)



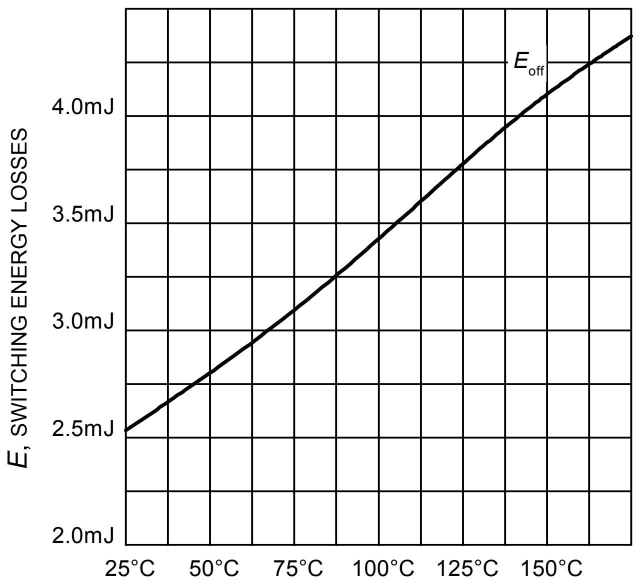
I_C, COLLECTOR CURRENT

Figure 13. Typical turn-off energy as a function of collector current
(inductive load, T_J=175°C, V_{CE}=600V, V_{GE}=0/15V, R_G=10Ω, Dynamic test circuit in Figure E)



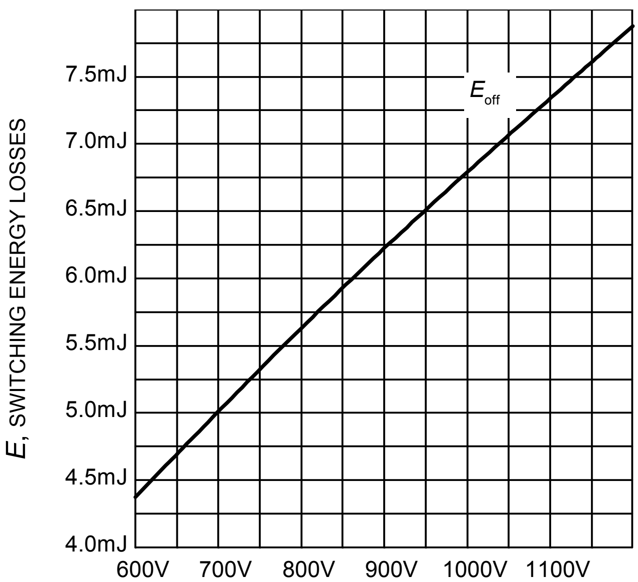
R_G, GATE RESISTOR

Figure 14. Typical turn-off energy as a function of gate resistor
(inductive load, T_J=175°C, V_{CE}=600V, V_{GE}=0/15V, I_C=30A, Dynamic test circuit in Figure E)



T_J, JUNCTION TEMPERATURE

Figure 15. Typical turn-off energy as a function of junction temperature
(inductive load, V_{CE}=600V, V_{GE}=0/15V, I_C=30A, R_G=10Ω, Dynamic test circuit in Figure E)



V_{CE}, COLLECTOR-EMITTER VOLTAGE

Figure 16. Typical turn-off energy as a function of collector emitter voltage
(inductive load, T_J=175°C, V_{GE}=0/15V, I_C=30A, R_G=10Ω, Dynamic test circuit in Figure E)

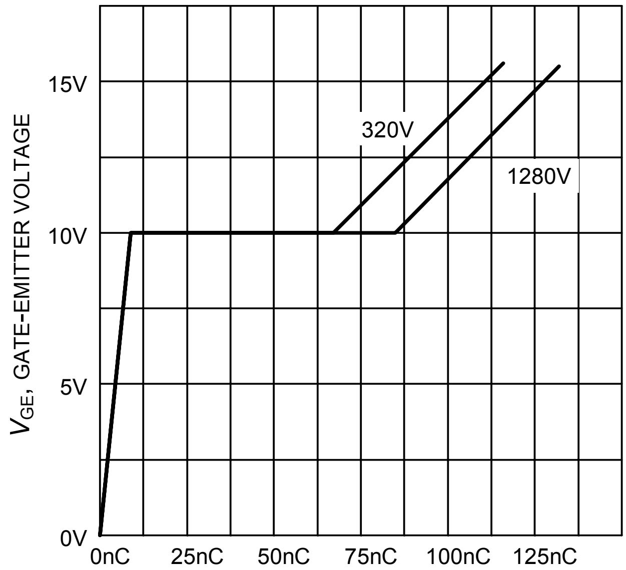


Figure 17. Typical gate charge
(I_C=30 A)

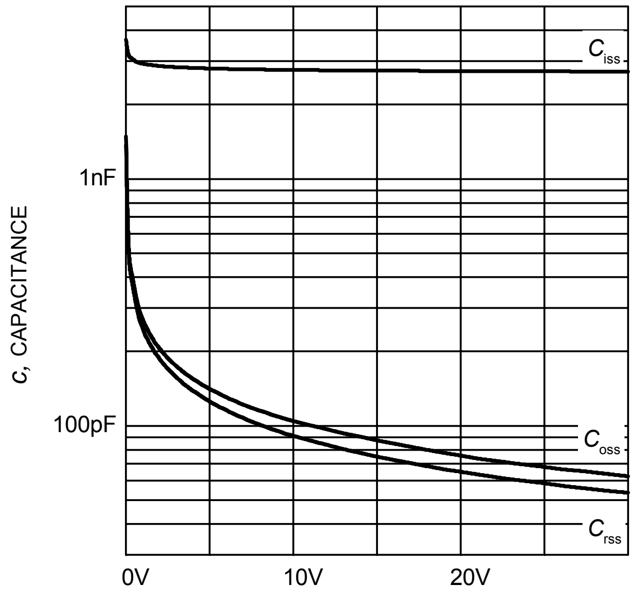
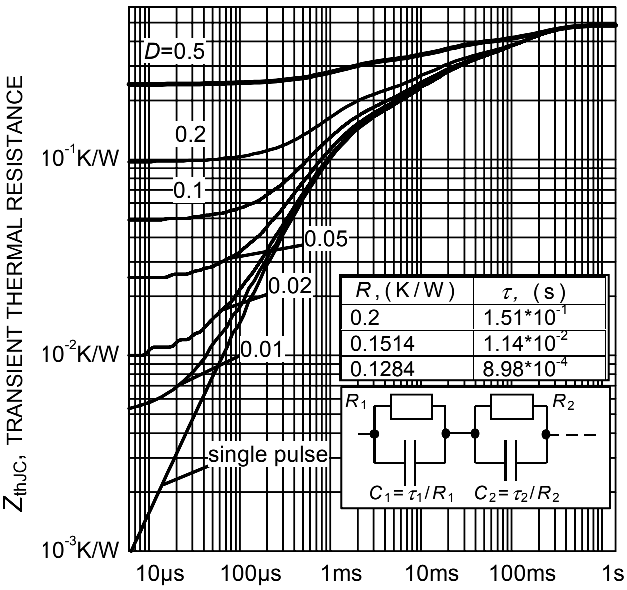
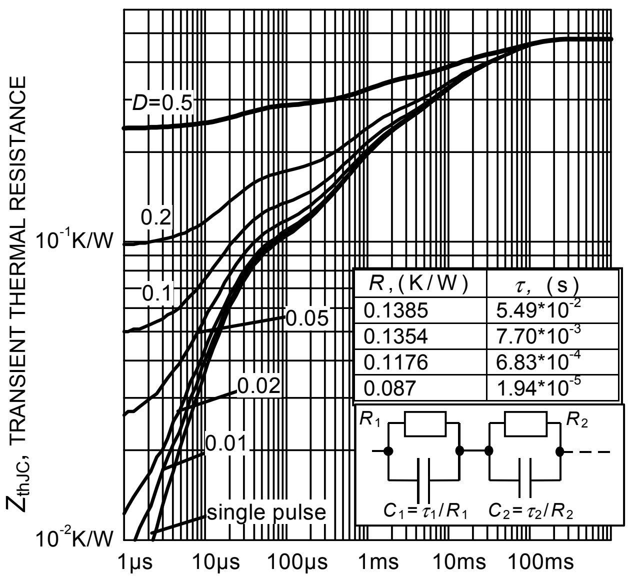


Figure 18. Typical capacitance as a function of collector-emitter voltage
(V_{GE}=0V, f = 1 MHz)



R, (K/W)	τ, (s)
0.2	$1.51*10^{-1}$
0.1514	$1.14*10^{-2}$
0.1284	$8.98*10^{-4}$

Figure 19. IGBT transient thermal resistance
($D = t_p / T$)



R, (K/W)	τ, (s)
0.1385	$5.49*10^{-2}$
0.1354	$7.70*10^{-3}$
0.1176	$6.83*10^{-4}$
0.087	$1.94*10^{-5}$

Figure 20. Diode transient thermal impedance as a function of pulse width
(D=t_P/T)

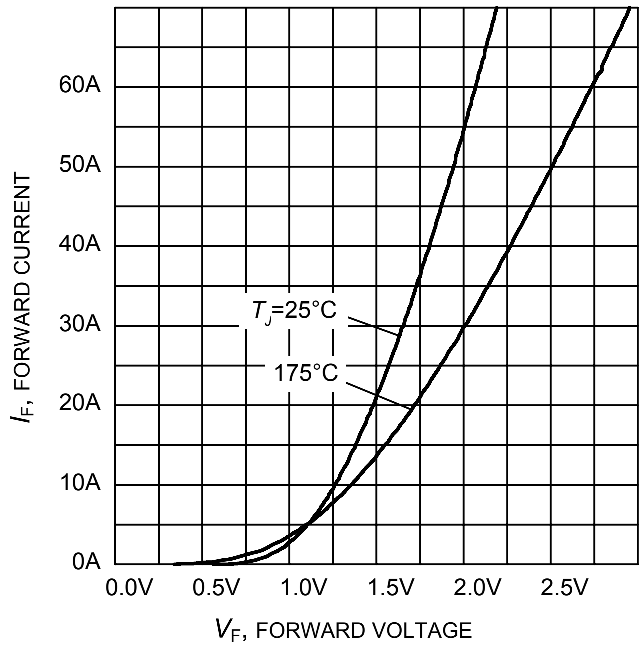


Figure 21. Typical diode forward current as a function of forward voltage

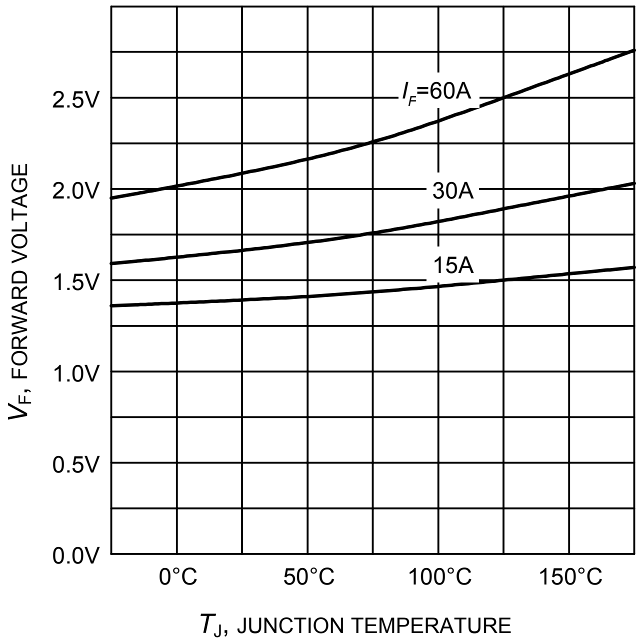
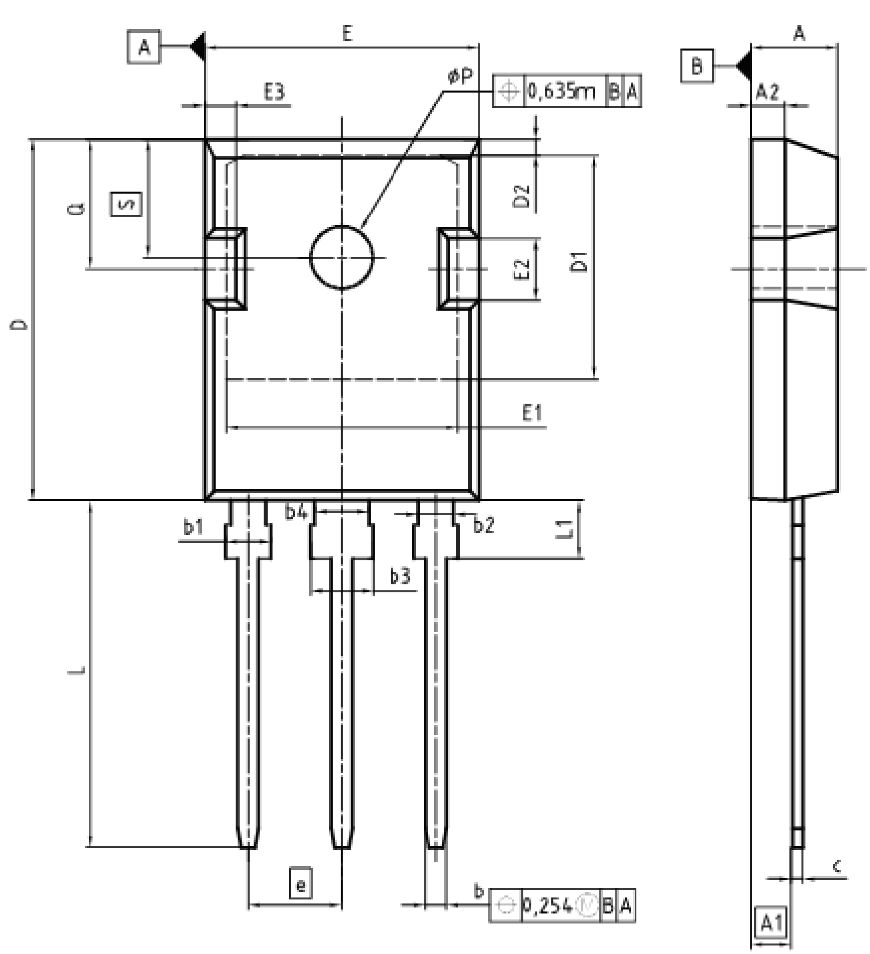


Figure 22. Typical diode forward voltage as a function of junction temperature

TO247-3



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.83	5.21	0.190	0.205
A1	2.27	2.54	0.089	0.100
A2	1.85	2.16	0.073	0.085
b	1.07	1.33	0.042	0.052
b1	1.90	2.41	0.075	0.095
b2	1.90	2.16	0.075	0.085
b3	2.87	3.38	0.113	0.133
b4	2.87	3.13	0.113	0.123
c	0.55	0.68	0.022	0.027
D	20.80	21.10	0.819	0.831
D1	16.25	17.65	0.640	0.695
D2	0.95	1.35	0.037	0.053
E	15.70	16.13	0.618	0.635
E1	13.10	14.15	0.516	0.557
E2	3.68	5.10	0.145	0.201
E3	1.00	2.60	0.039	0.102
e	5.44		0.214	
N	3		3	
L	19.80	20.32	0.780	0.800
L1	4.10	4.47	0.161	0.176
øP	3.50	3.70	0.138	0.146
Q	5.49	6.00	0.216	0.236
S	6.04	6.30	0.238	0.248

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SCALE

EUROPEAN PROJECTION

ISSUE DATE
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REVISION
04

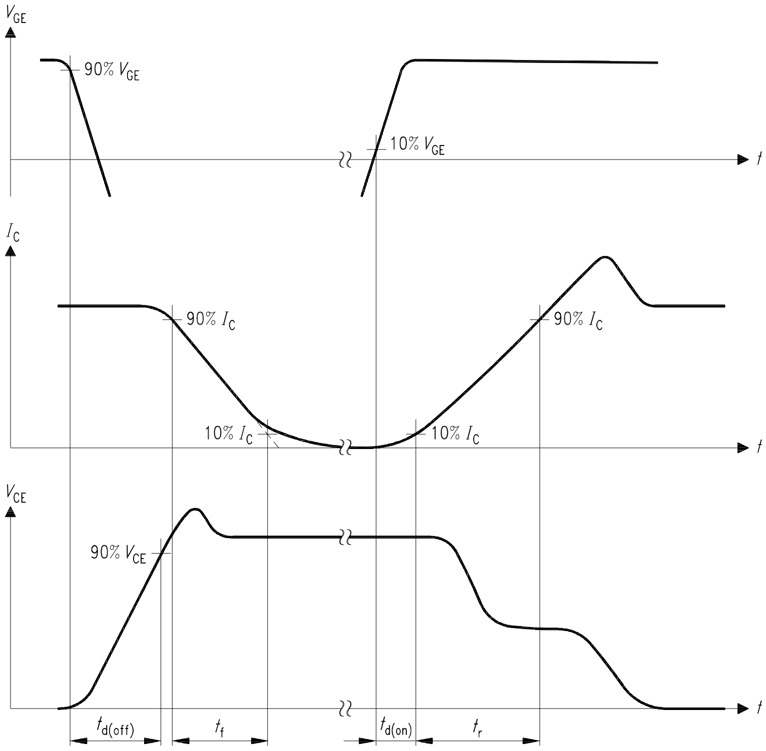

Figure A. Definition of switching times

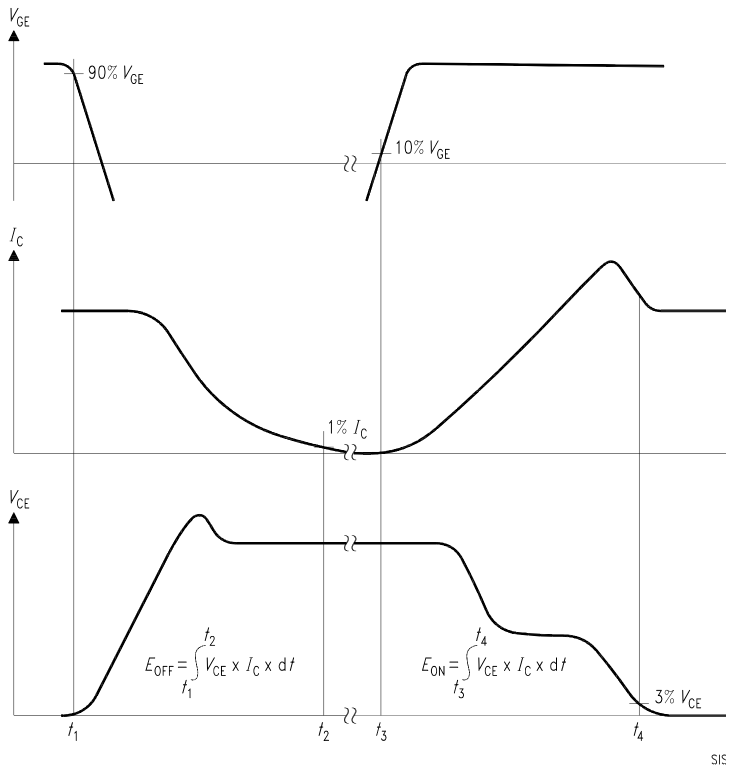

Figure B. Definition of switching losses

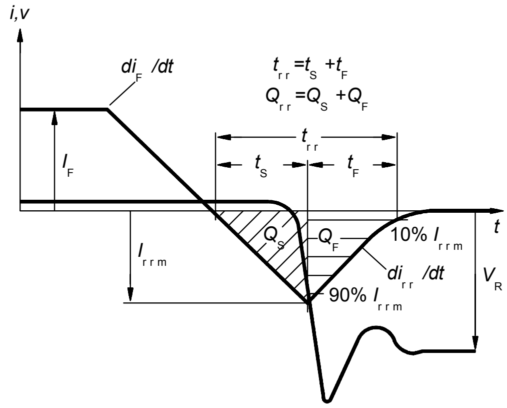

Figure C. Definition of diodes switching characteristics

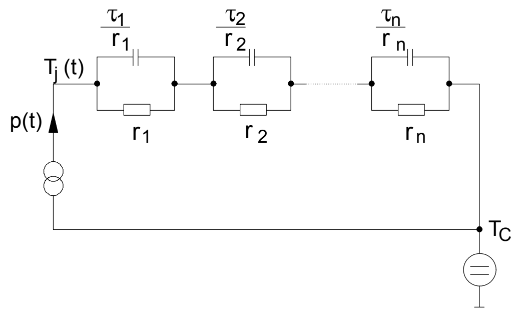

Figure D. Thermal equivalent circuit

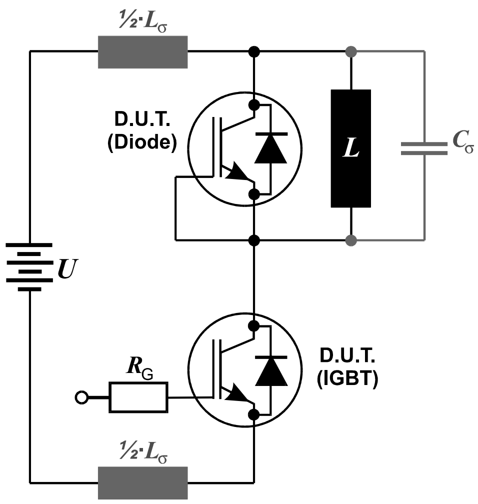

Figure E. Dynamic test circuit

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Příloha číslo 3

Katalogový list: Integrovaný obvod TL494

MOTOROLA

TL494

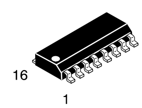
SWITCHMODE™ Pulse Width Modulation Control Circuit

The TL494 is a fixed frequency, pulse width modulation control circuit designed primarily for SWITCHMODE power supply control.

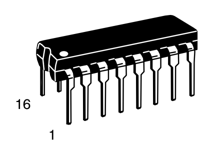
- Complete Pulse Width Modulation Control Circuitry
- On–Chip Oscillator with Master or Slave Operation
- On–Chip Error Amplifiers
- On–Chip 5.0 V Reference
- Adjustable Deadtime Control
- Uncommitted Output Transistors Rated to 500 mA Source or Sink
- Output Control for Push–Pull or Single–Ended Operation
- Undervoltage Lockout

SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUIT

SEMICONDUCTOR TECHNICAL DATA

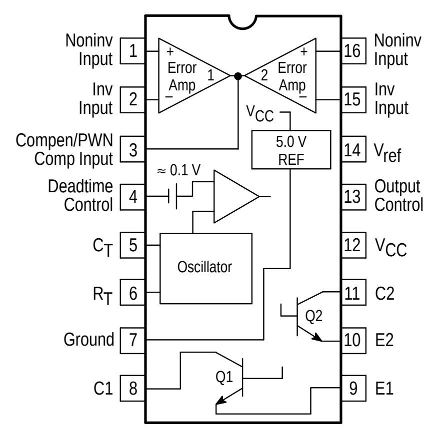


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



N SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	TL494C	TL494I	Unit
Power Supply Voltage	V_{CC}	42		V
Collector Output Voltage	V_{C1}, V_{C2}	42		V
Collector Output Current (Each transistor) (Note 1)	I_{C1}, I_{C2}	500		mA
Amplifier Input Voltage Range	V_{IR}	–0.3 to +42		V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000		mW
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	80		°C/W
Operating Junction Temperature	T_J	125		°C
Storage Temperature Range	T_{stg}	–55 to +125		°C
Operating Ambient Temperature Range TL494C TL494I	T_A	 0 to +70 –25 to +85		°C
Derating Ambient Temperature	T_A	45		°C

NOTE: 1. Maximum thermal limits must be observed.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
TL494CD	T_A = 0° to +70°C	SO–16
TL494CN		Plastic
TL494IN	T_A = – 25° to +85°C	Plastic

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	–	30	40	V
Collector Output Current (Each transistor)	I_{C1}, I_{C2}	–	–	200	mA
Amplified Input Voltage	V_{in}	–0.3	–	V_{CC} – 2.0	V
Current Into Feedback Terminal	I_{fb}	–	–	0.3	mA
Reference Output Current	I_{ref}	–	–	10	mA
Timing Resistor	R_T	1.8	30	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	µF
Oscillator Frequency	f_{osc}	1.0	40	200	kHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted.)

For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Voltage (I_O = 1.0 mA)	V_{ref}	4.75	5.0	5.25	V
Line Regulation (V_{CC} = 7.0 V to 40 V)	Reg_{line}	–	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	–	3.0	15	mV
Short Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	35	75	mA
OUTPUT SECTION					
Collector Off–State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	–	2.0	100	µA
Emitter Off–State Current V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	–	–	–100	µA
Collector–Emitter Saturation Voltage (Note 2)					V
Common–Emitter (V_E = 0 V, I_C = 200 mA)	$V_{sat(C)}$	–	1.1	1.3	
Emitter–Follower (V_C = 15 V, I_E = –200 mA)	$V_{sat(E)}$	–	1.5	2.5	
Output Control Pin Current					
Low State (V_{OC} ≤ 0.4 V)	I_{OCL}	–	10	–	µA
High State (V_{OC} = V_{ref})	I_{OCH}	–	0.2	3.5	mA
Output Voltage Rise Time	t_r				ns
Common–Emitter (See Figure 12)		–	100	200	
Emitter–Follower (See Figure 13)		–	100	200	
Output Voltage Fall Time	t_f				ns
Common–Emitter (See Figure 12)		–	25	100	
Emitter–Follower (See Figure 13)		–	40	100	

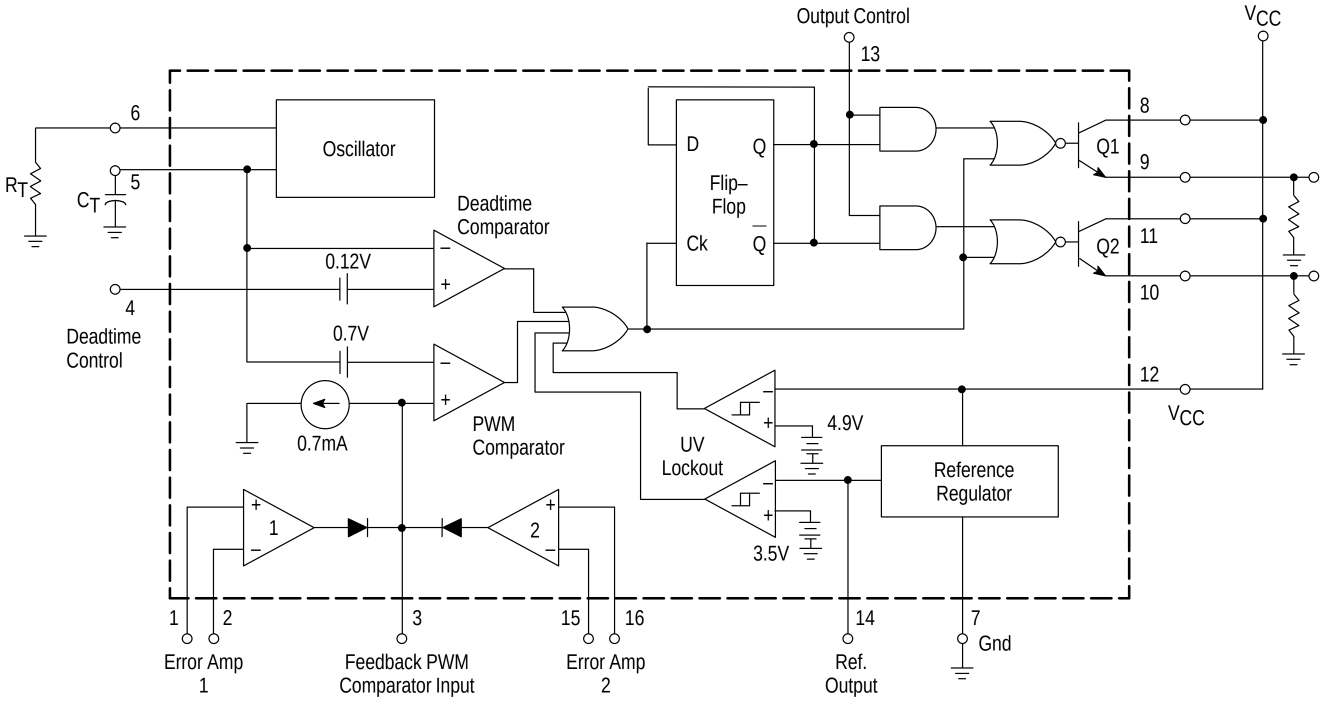
NOTE: 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ, unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION					
Input Offset Voltage ($V_{O\ (Pin\ 3)}$ = 2.5 V)	V_{IO}	–	2.0	10	mV
Input Offset Current ($V_{O\ (Pin\ 3)}$ = 2.5 V)	I_{IO}	–	5.0	250	nA
Input Bias Current ($V_{O\ (Pin\ 3)}$ = 2.5 V)	I_{IB}	–	–0.1	–1.0	μA
Input Common Mode Voltage Range (V_{CC} = 40 V, T_A = 25°C)	V_{ICR}	–0.3 to V_{CC}–2.0			V
Open Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	–	dB
Unity–Gain Crossover Frequency (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	$f_{C–}$	–	350	–	kHz
Phase Margin at Unity–Gain (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	ϕ_m	–	65	–	deg.
Common Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90	–	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	–	100	–	dB
Output Sink Current ($V_{O\ (Pin\ 3)}$ = 0.7 V)	$I_{O–}$	0.3	0.7	–	mA
Output Source Current ($V_{O\ (Pin\ 3)}$ = 3.5 V)	I_{O+}	2.0	–4.0	–	mA
PWM COMPARATOR SECTION (Test Circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	–	2.5	4.5	V
Input Sink Current ($V_{(Pin\ 3)}$ = 0.7 V)	$I_{I–}$	0.3	0.7	–	mA
DEADTIME CONTROL SECTION (Test Circuit Figure 11)					
Input Bias Current (Pin 4) ($V_{Pin\ 4}$ = 0 V to 5.25 V)	$I_{IB\ (DT)}$	–	–2.0	–10	μA
Maximum Duty Cycle, Each Output, Push–Pull Mode	DC_{max}				%
($V_{Pin\ 4}$ = 0 V, C_T = 0.01 μF, R_T = 12 kΩ)		45	48	50	
($V_{Pin\ 4}$ = 0 V, C_T = 0.001 μF, R_T = 30 kΩ)		–	45	50	
Input Threshold Voltage (Pin 4)	V_{th}				V
(Zero Duty Cycle)		–	2.8	3.3	
(Maximum Duty Cycle)		0	–	–	
OSCILLATOR SECTION					
Frequency (C_T = 0.001 μF, R_T = 30 kΩ)	f_{osc}	–	40	–	kHz
Standard Deviation of Frequency* (C_T = 0.001 μF, R_T = 30 kΩ)	σf_{osc}	–	3.0	–	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	Δf_{osc} (ΔV)	–	0.1	–	%
Frequency Change with Temperature (ΔT_A = T_{low} to T_{high}) (C_T = 0.01 μF, R_T = 12 kΩ)	Δf_{osc} (ΔT)	–	–	12	%
UNDERVOLTAGE LOCKOUT SECTION					
Turn–On Threshold (V_{CC} increasing, I_{ref} = 1.0 mA)	V_{th}	5.5	6.43	7.0	V
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, All other inputs and outputs open)	I_{CC}				mA
(V_{CC} = 15 V)		–	5.5	10	
(V_{CC} = 40 V)		–	7.0	15	
Average Supply Current (C_T = 0.01 μF, R_T = 12 kΩ, $V_{(Pin\ 4)}$ = 2.0 V) (V_{CC} = 15 V) (See Figure 12)		–	7.0	–	mA

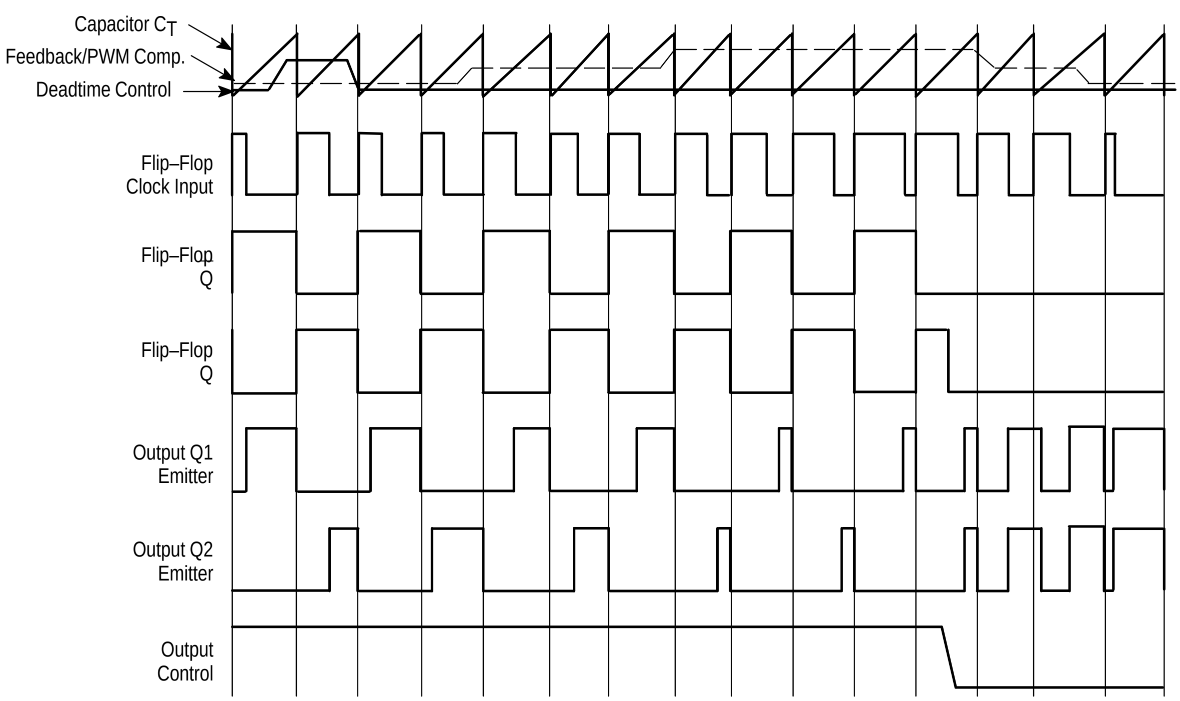
* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \sqrt{\dfrac{\sum_{n=1}^{N} (X_n - \bar{X})^2}{N - 1}}$

Figure 1. Representative Block Diagram



This device contains 46 active transistors.

Figure 2. Timing Diagram



APPLICATIONS INFORMATION

Description

The TL494 is a fixed–frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal–linear sawtooth oscillator is frequency–programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip–flop clock–input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control–signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the deadtime control, the error amplifier inputs, or the feedback input. The deadtime control comparator has an effective 120 mV input offset which limits the minimum output deadtime to approximately the first 4% of the sawtooth–cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional deadtime may be imposed on the output by setting the deadtime–control input to a fixed voltage, ranging between 0 V to 3.3 V.

Functional Table

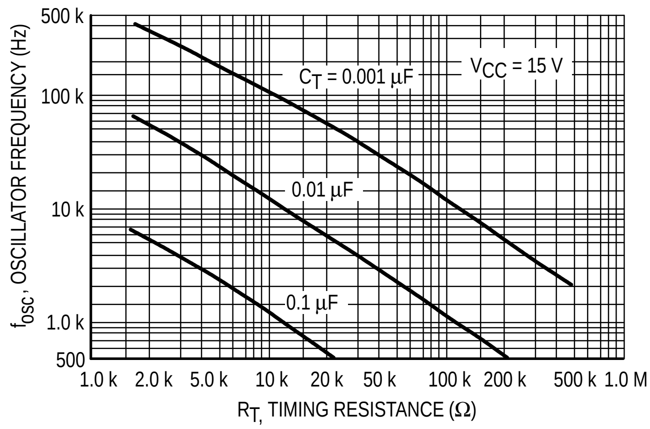
Input/Output Controls	Output Function	$\frac{f_{out}}{f_{osc}}$ =
Grounded	Single–ended PWM @ Q1 and Q2	1.0
@ V_{ref}	Push–pull Operation	0.5

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on–time, established by the deadtime control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common mode input range from –0.3 V to (V_{CC} – 2V), and may be used to sense power–supply output voltage and current. The error–amplifier outputs are active high and are ORed together at the noninverting input of the pulse–width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor C_T is discharged, a positive pulse is generated on the output of the deadtime comparator, which clocks the pulse–steering flip–flop and inhibits the output transistors, Q1 and Q2. With the output–control connected to the reference line, the pulse–steering flip–flop directs the modulated pulses to each of the two output transistors alternately for push–pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single–ended operation with a maximum on–time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output–drive currents are required for single–ended operation, Q1 and Q2 may be connected in parallel, and the output–mode pin must be tied to ground to disable the flip–flop. The output frequency will now be equal to that of the oscillator.

The TL494 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of ±5.0% with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to 70°C.

Figure 3. Oscillator Frequency versus Timing Resistance



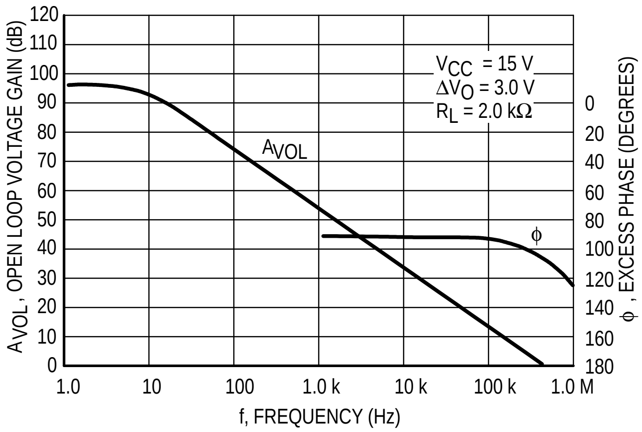


Figure 4. Open Loop Voltage Gain and Phase versus Frequency

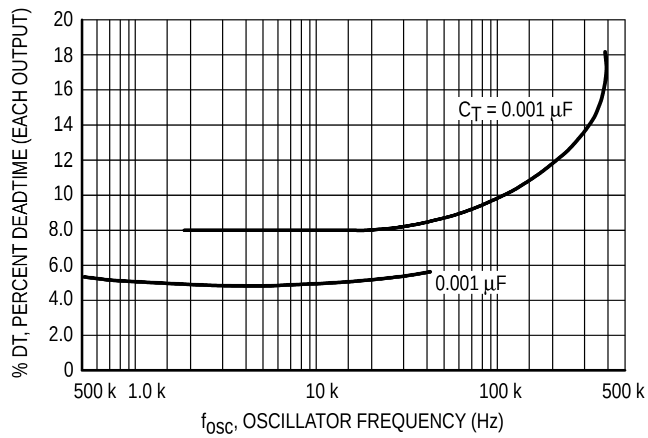


Figure 5. Percent Deadtime versus Oscillator Frequency

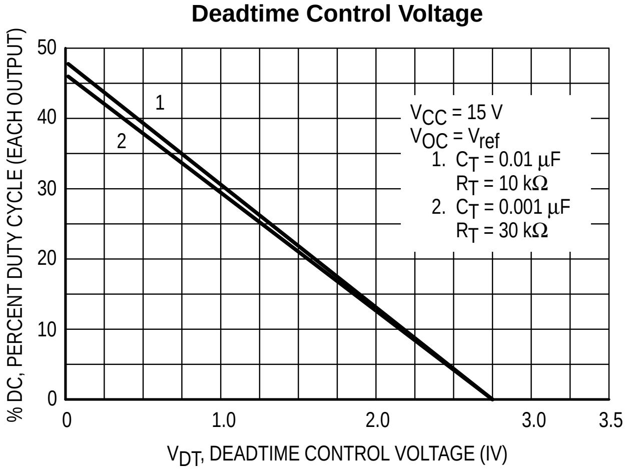


Figure 6. Percent Duty Cycle versus Deadtime Control Voltage

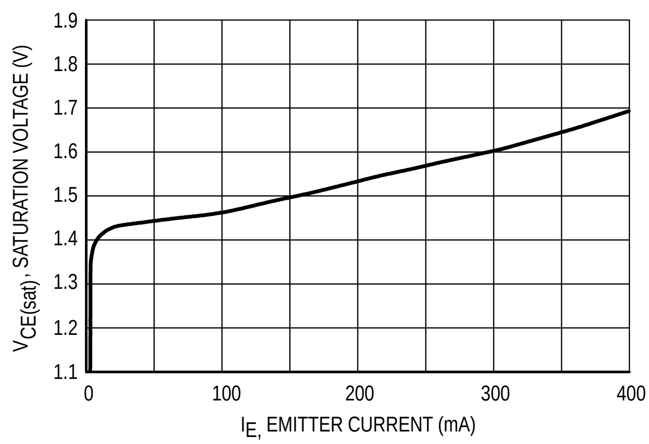


Figure 7. Emitter–Follower Configuration Output Saturation Voltage versus Emitter Current

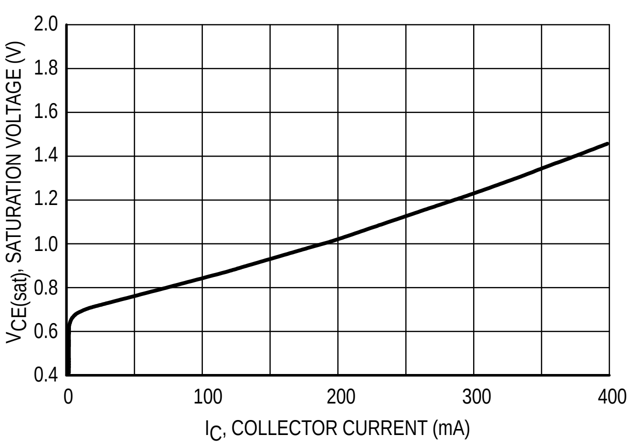


Figure 8. Common–Emitter Configuration Output Saturation Voltage versus Collector Current

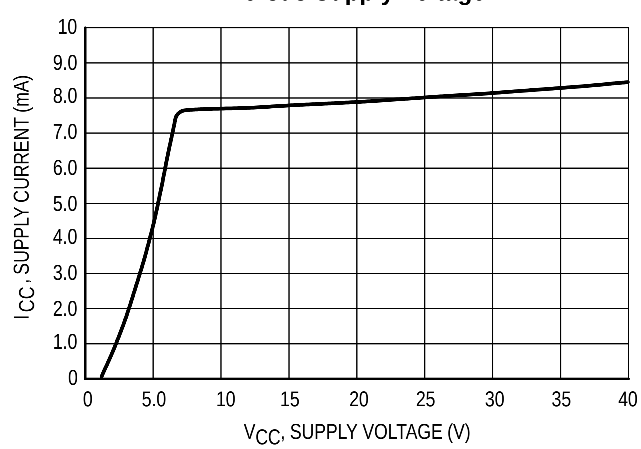


Figure 9. Standby Supply Current versus Supply Voltage

Figure 10. Error–Amplifier Characteristics

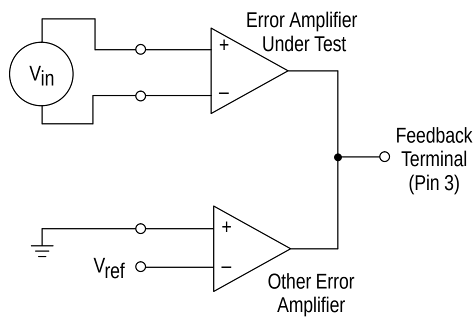


Figure 11. Deadtime and Feedback Control Circuit

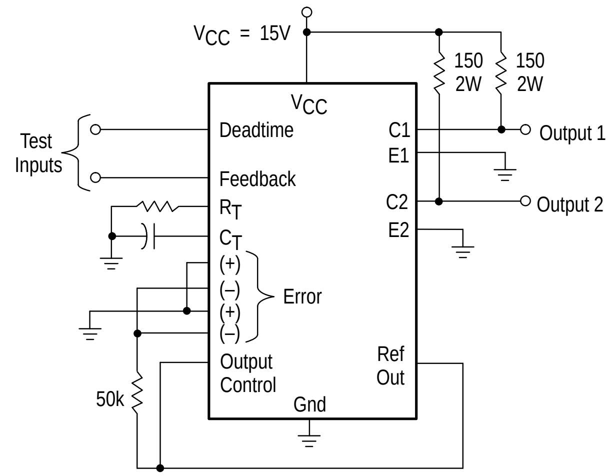


Figure 12. Common–Emitter Configuration Test Circuit and Waveform

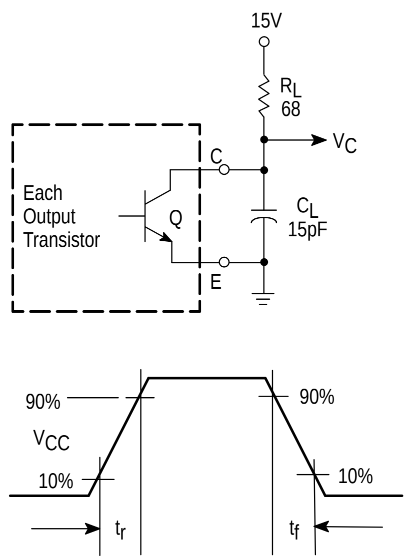


Figure 13. Emitter–Follower Configuration Test Circuit and Waveform

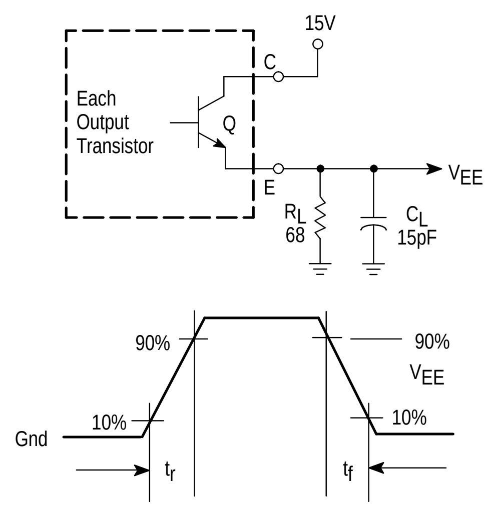


Figure 14. Error–Amplifier Sensing Techniques

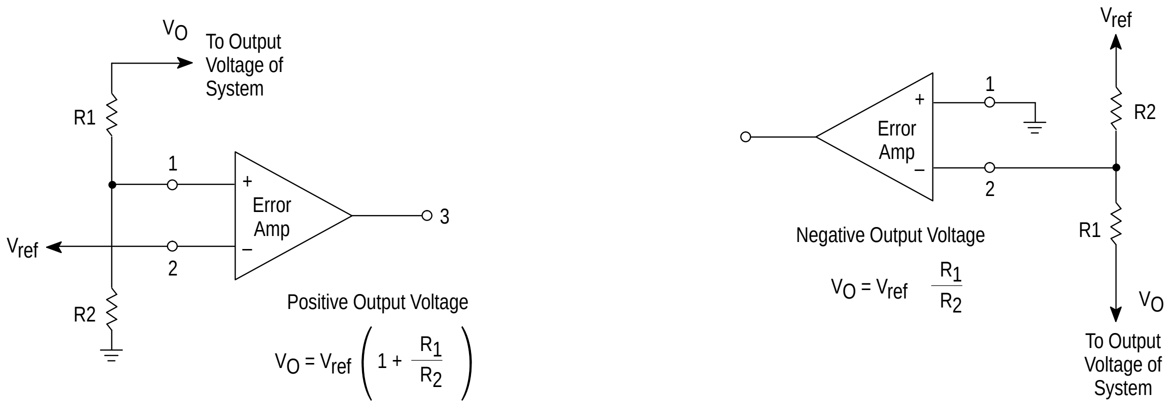
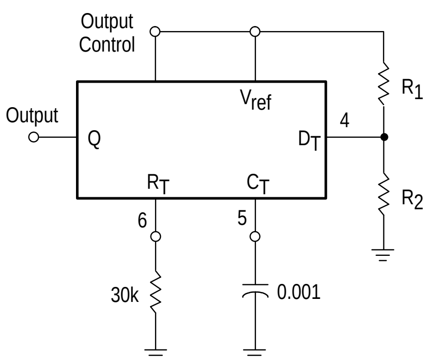


Figure 15. Deadtime Control Circuit



$$\text{Max. \% on Time, each output} \approx 45 - \left(\frac{80}{1 + \frac{R1}{R2}}\right)$$

Figure 16. Soft–Start Circuit

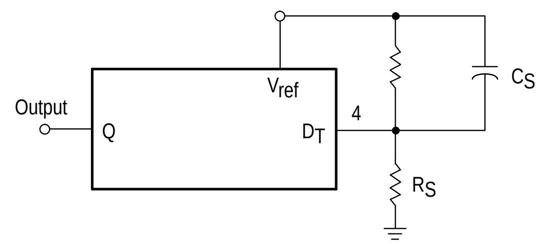


Figure 17. Output Connections for Single–Ended and Push–Pull Configurations

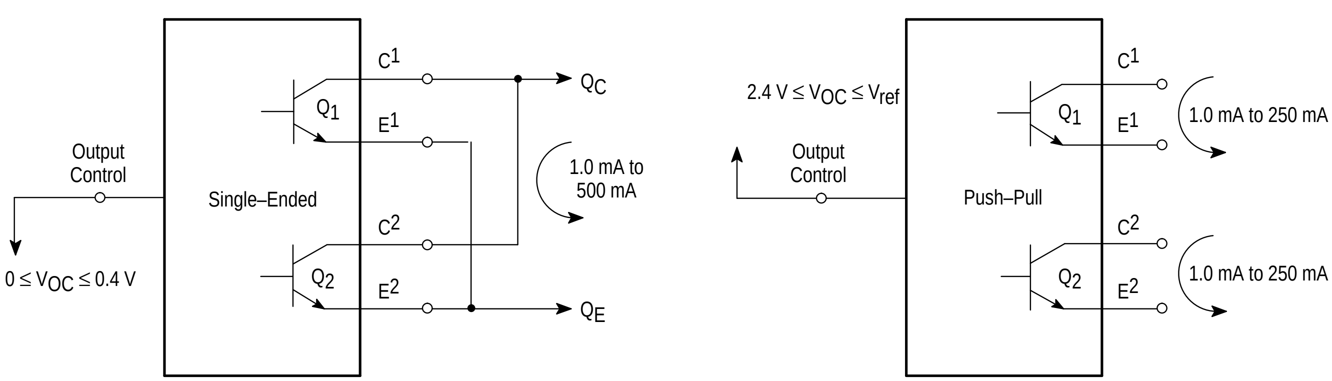


Figure 18. Slaving Two or More Control Circuits

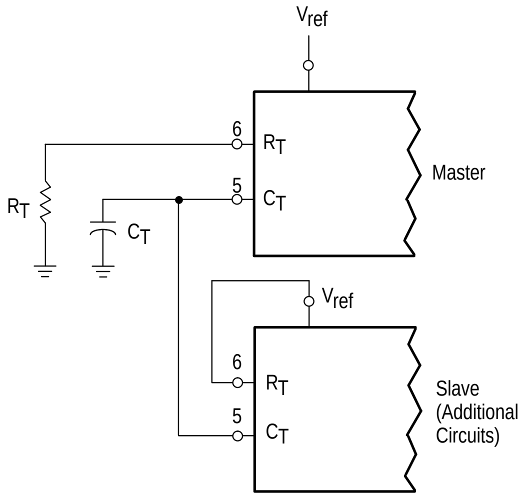


Figure 19. Operation with V_{in} > 40 V Using External Zener

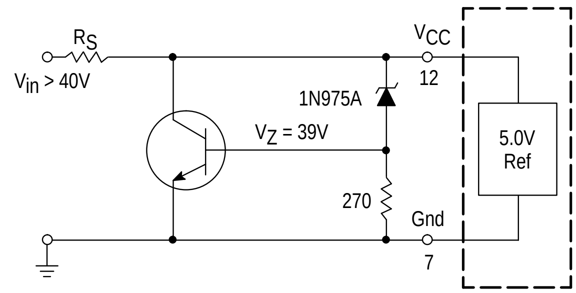
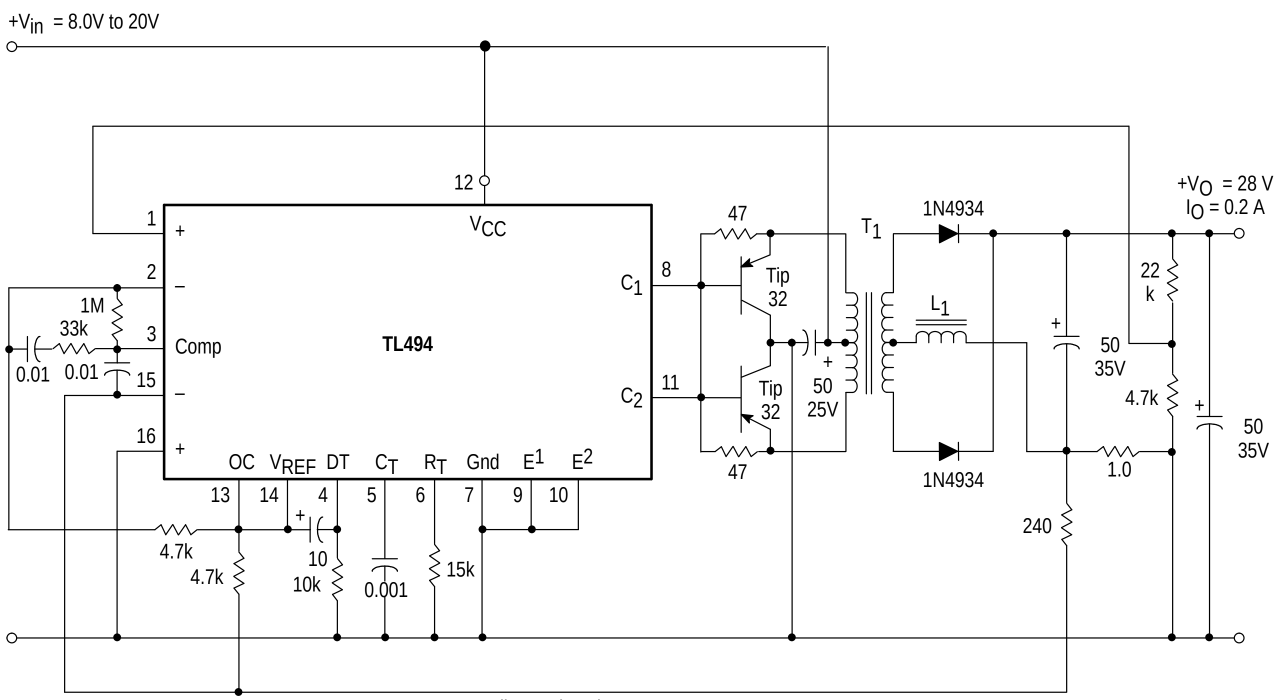


Figure 20. Pulse Width Modulated Push–Pull Converter

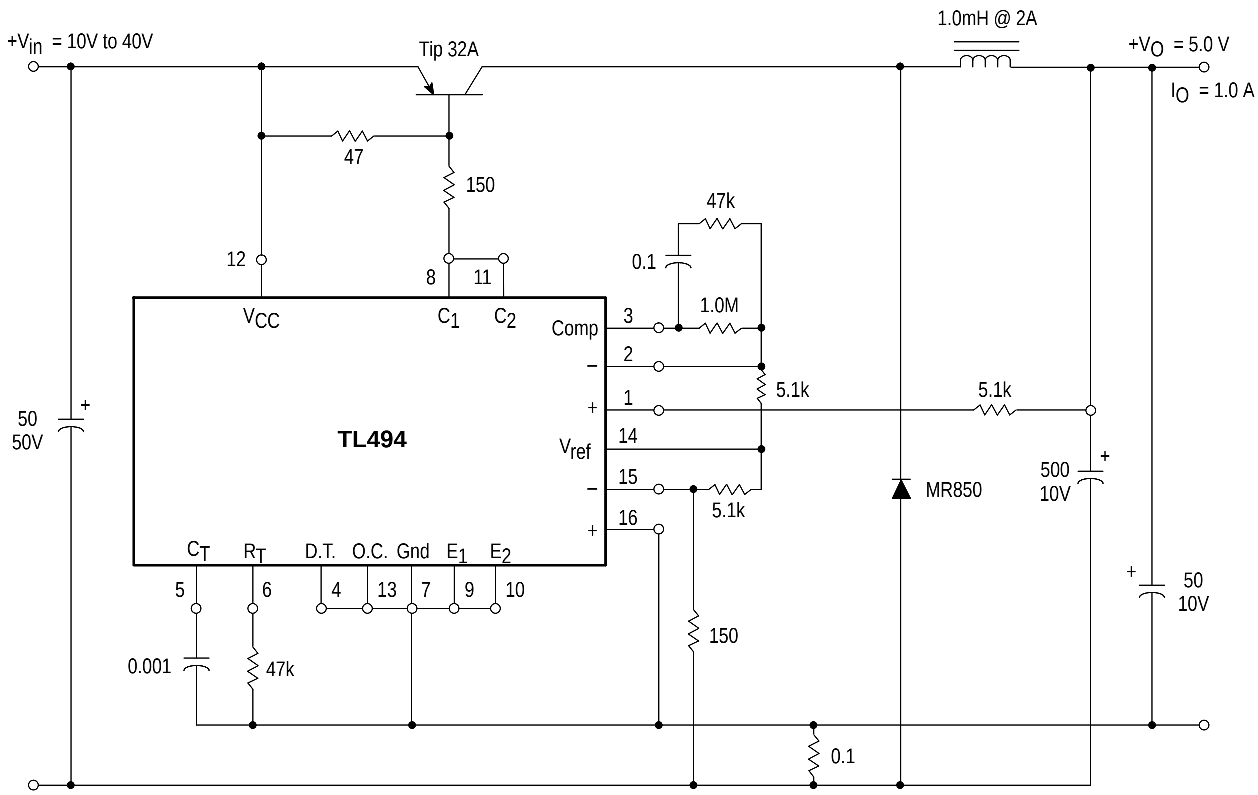


All capacitors in µF

Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 40 V	14 mV 0.28%
Load Regulation	V_{in} = 28 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 28 V, I_O = 1.0 A	65 mV pp P.A.R.D.
Short Circuit Current	V_{in} = 28 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 28 V, I_O = 1.0 A	71%

L1 – 3.5 mH @ 0.3 A
T1 – Primary: 20T C.T. #28 AWG
Secondary: 12OT C.T. #36 AWG
Core: Ferroxcube 1408P–L00–3CB

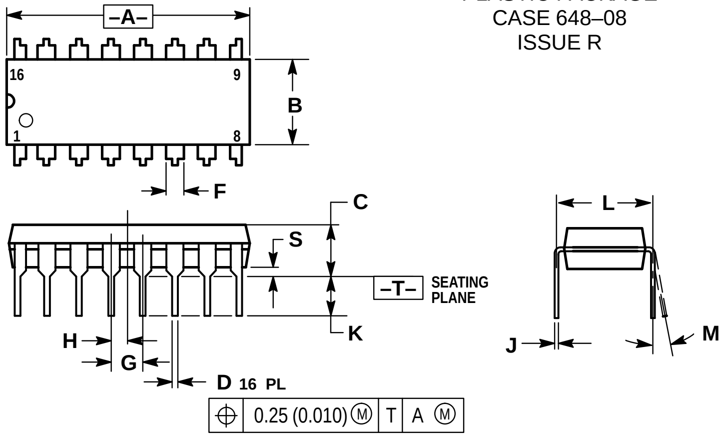
Figure 21. Pulse Width Modulated Step–Down Converter



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 40 V	3.0 mV 0.01%
Load Regulation	V_{in} = 12.6 V, I_O = 0.2 mA to 200 mA	5.0 mV 0.02%
Output Ripple	V_{in} = 12.6 V, I_O = 200 mA	40 mV pp P.A.R.D.
Short Circuit Current	V_{in} = 12.6 V, R_L = 0.1 Ω	250 mA
Efficiency	V_{in} = 12.6 V, I_O = 200 mA	72%

OUTLINE DIMENSIONS

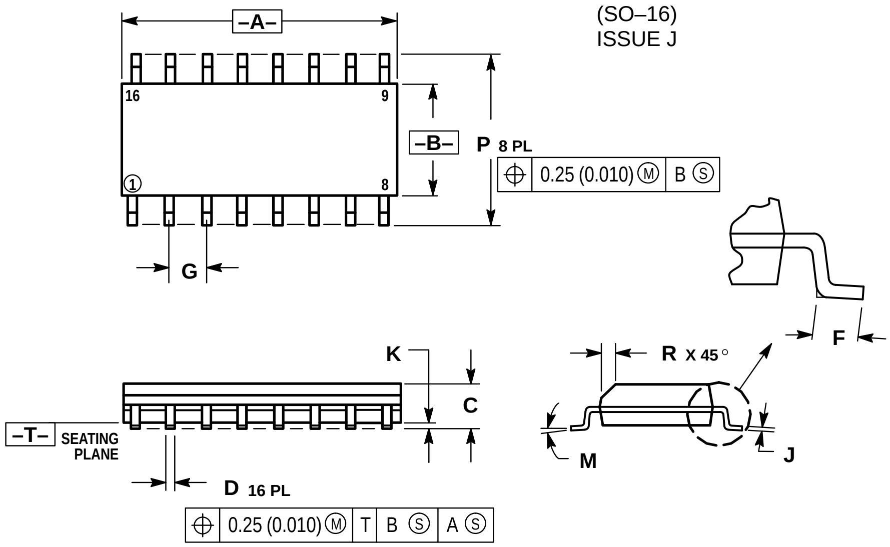
N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC PACKAGE
CASE 751B–05
(SO–16)
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

Příloha číslo 4

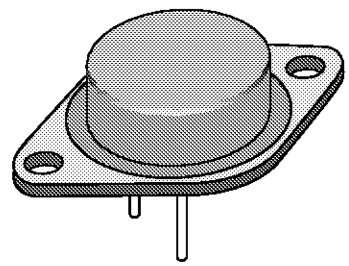
Katalogový list: Regulátory napětí L78S00

SGS-THOMSON MICROELECTRONICS

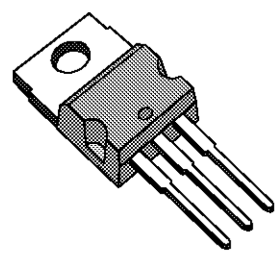
L78S00 SERIES

2A POSITIVE VOLTAGE REGULATORS

- OUTPUT CURRENT TO 2A
- OUTPUT VOLTAGES OF 5 ; 7.5 ; 9 ; 10 ; 12 ; 15 ; 18 ; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR SOA PROTECTION



TO-3

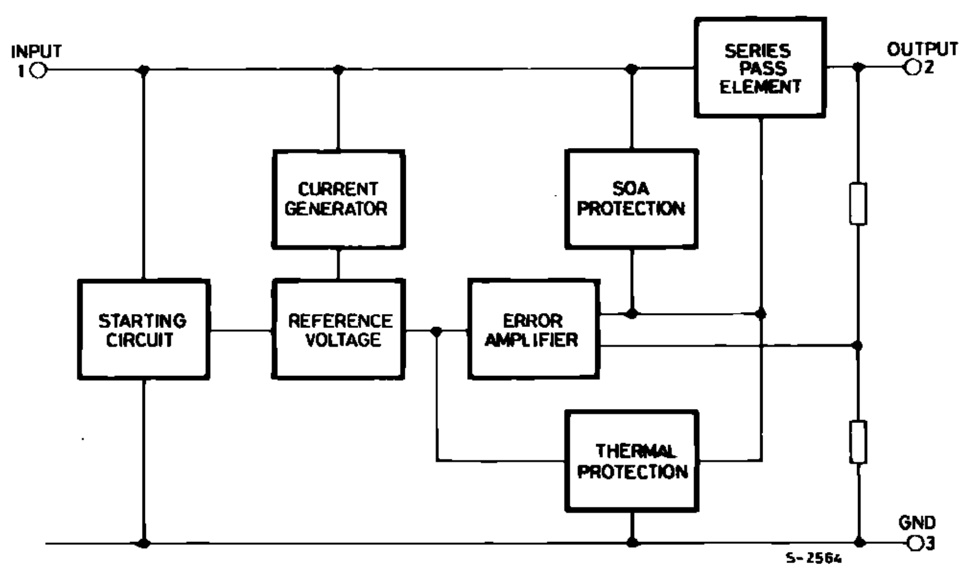


TO-220

DESCRIPTION

The L78S00 series of three-terminal positive regulators is available in TO-220 and TO-3 packages and with several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 2A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

BLOCK DIAGRAM



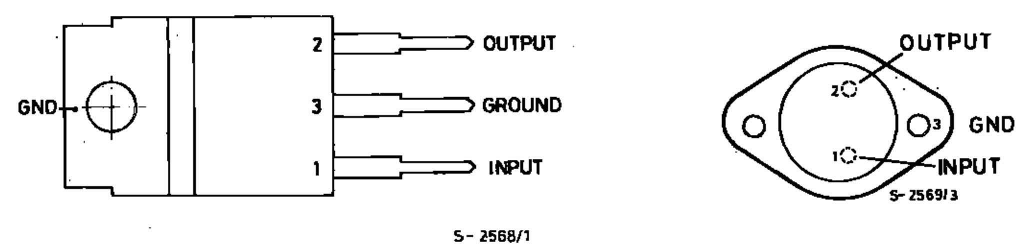
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage (for V_o = 5 to 18V) (for V_o = 24V)	35 40	V V
I_o	Output Current	Internally limited	
P_{tot}	Power Dissipation	Internally limited	
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_{op}	Operating Junction Temperature (for **L78S00**) (for **L78S00C**)	– 55 to + 150 0 to + 150	°C °C

THERMAL DATA

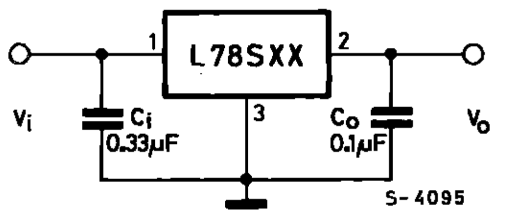
		TO-220	TO-3	
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case Max	3	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient Max	50	35	°C/W

CONNECTION DIAGRAMS AND ORDERING NUMBERS (top views)

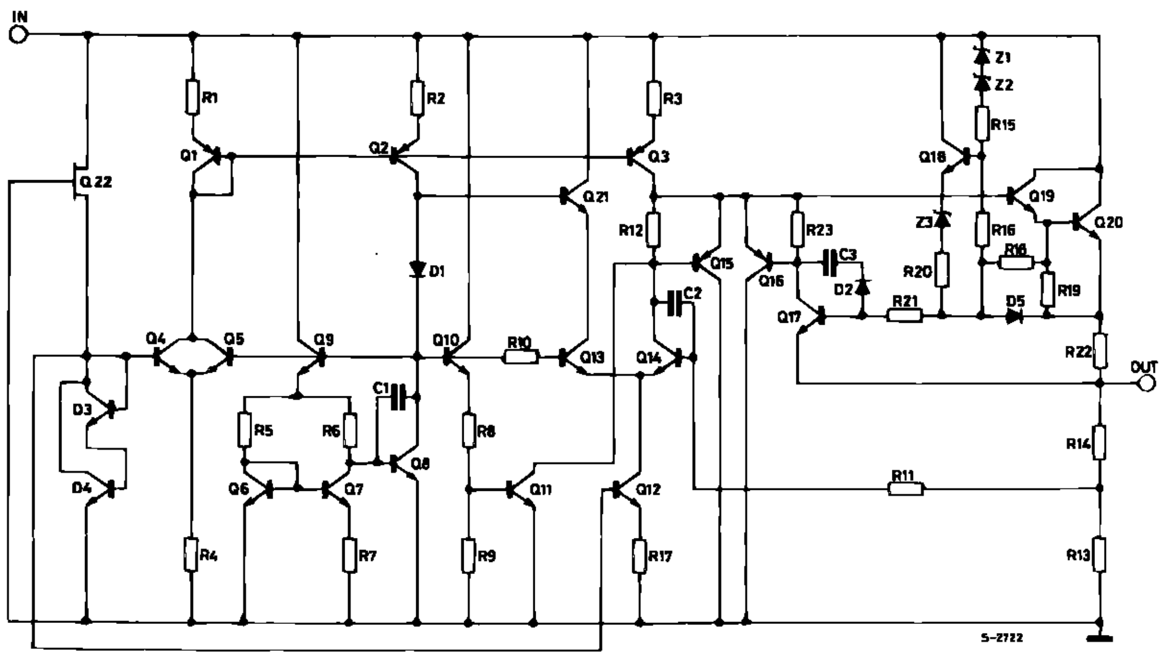


Type	TO-220	TO-3	Output Voltage
L78S05		L78S05T	5 V
L78S05C	L78S05CV	L78S05CT	5 V
L78S75		L78S75T	7.5V
L78S75C	L78S75CV	L78S75CT	7.5V
L78S09		L78S09T	9 V
L78S09C	L78S09CV	L78S09CT	9 V
L78S10		L78S10T	10V
L78S10C	L78S10CV	L78S10CT	10V
L78S12		L78S12T	12V
L78S12C	L78S12CV	L78S12CT	12V
L78S15		L78S15T	15V
L78S15C	L78S15CV	L78S15CT	15V
L78S18		L78S18T	18V
L78S18C	L78S18CV	L78S18CT	18V
L78S24		L78S24T	24V
L78S24C	L78S24CV	L78S24CT	24V

APPLICATION CIRCUIT



SCHEMATIC DIAGRAM



TEST CIRCUITS

Figure 1 : DC Parameters.

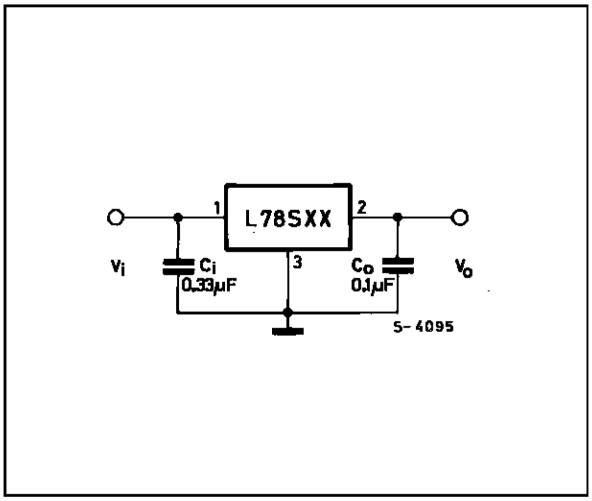


Figure 2 : Load Regulation.

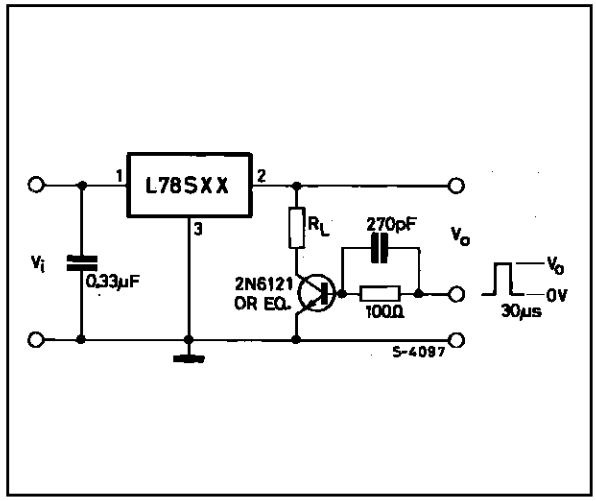
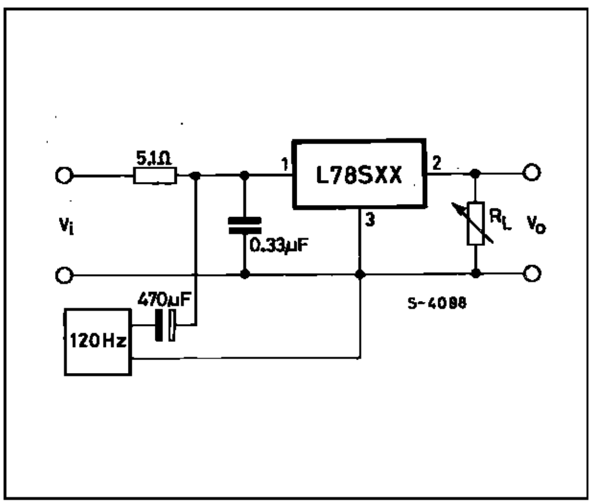


Figure 3 : Ripple Rejection.



ELECTRICAL CHARACTERISTICS FOR L78S05 (refer to the test circuits, T_j = 25 °C, V_i = 10V, I_o = 500 mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage		4.8	5	5.2	V
V_o	Output Voltage	I_o = 1 A V_i = 7 V	4.75	5	5.25	V
ΔV_o	Line Regulation	V_i = 7 to 25 V V_i = 8 to 25 V			100 50	mV mV
ΔV_o	Load Regulation	I_o = 20 mA to 2 A			100	mV
I_d	Quiescent Current				8	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA to 1A			0.5	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA V_i = 7 to 25 V			1.3	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA T_j = -55 to 150 °C		-1.1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz		40		μV
SVR	Supply Voltage Rejection	f = 120 Hz	60			dB
V_i	Operating Input Voltage	$I_o \leq$ 1.5 A	8			V
R_o	Output Resistance	f = 1KHz		17		mΩ
I_{sc}	Short Circuit Current	V_i = 27 V		500		mA
I_{scp}	Short Circuit Peack Current			3		A

ELECTRICAL CHARACTERISTICS FOR L78S75 (refer to the test circuits, T_j = 25 °C, V_i = 12.5V, I_o = 500 mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage		7.15	7.5	7.9	V
V_o	Output Voltage	I_o = 1 A V_i = 9.5 V	7.1	7.5	7.95	V
ΔV_o	Line Regulation	V_i = 9.5 to 25 V V_i = 10.5 to 20 V			120 60	mV mV
ΔV_o	Load Regulation	I_o = 20 mA to 2 A			120	mV
I_d	Quiescent Current				8	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA to 1A			0.5	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA V_i = 9.5 to 25 V			1.3	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA T_j = -55 to 150 °C		-0.8		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz		52		μV
SVR	Supply Voltage Rejection	f = 120 Hz	54			dB
V_i	Operating Input Voltage	$I_o \leq$ 1.5 A	10.5			V
R_o	Output Resistance	f = 1KHz		16		mΩ
I_{sc}	Short Circuit Current	V_i = 27 V		500		mA
I_{scp}	Short Circuit Peack Current			3		A

ELECTRICAL CHARACTERISTICS FOR L78S09 (refer to the test circuits, T_j = 25 °C, V_i = 14V, I_o = 500 mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage		8.65	9	9.35	V
V_o	Output Voltage	I_o = 1 A V_i = 11 V	8.6	9	9.4	V
ΔV_o	Line Regulation	V_i = 11 to 25 V V_i = 11 to 20 V			130 65	mV mV
ΔV_o	Load Regulation	I_o = 20 mA to 2 A			130	mV
I_d	Quiescent Current				8	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA to 1A			0.5	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA V_i = 11 to 25 V			1.3	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA T_j = -55 to 150 °C		-1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz		60		μV
SVR	Supply Voltage Rejection	f = 120 Hz	53			dB
V_i	Operating Input Voltage	$I_o \leq$ 1.5 A	12			V
R_o	Output Resistance	f = 1KHz		17		mΩ
I_{sc}	Short Circuit Current	V_i = 27 V		500		mA
I_{scp}	Short Circuit Peack Current			3		A

ELECTRICAL CHARACTERISTICS FOR L78S10 (refer to the test circuits, T_j = 25 °C, V_i = 15V, I_o = 500 mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage		9.5	10	10.5	V
V_o	Output Voltage	I_o = 1 A V_i = 12.5 V	9.4	10	10.6	V
ΔV_o	Line Regulation	V_i = 12.5 to 30 V V_i = 14 to 22 V			200 100	mV mV
ΔV_o	Load Regulation	I_o = 20 mA to 2 A			150	mV
I_d	Quiescent Current				8	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA to 1A			0.5	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA V_i = 12.5 to 30 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA T_j = -55 to 150 °C		-1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz		65		μV
SVR	Supply Voltage Rejection	f = 120 Hz	53			dB
V_i	Operating Input Voltage	$I_o \leq$ 1.5 A	13			V
R_o	Output Resistance	f = 1KHz		17		mΩ
I_{sc}	Short Circuit Current	V_i = 27 V		500		mA
I_{scp}	Short Circuit Peack Current			3		A

ELECTRICAL CHARACTERISTICS FOR L78S12 (refer to the test circuits, T_j = 25 ^oC, V_i = 19V, I_o = 500 mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage		11.5	12	12.5	V
V_o	Output Voltage	I_o = 1 A V_i = 14.5 V	11.4	12	12.6	V
ΔV_o	Line Regulation	V_i = 14.5 to 30 V V_i = 16 to 22 V			240 120	mV mV
ΔV_o	Load Regulation	I_o = 20 mA to 2 A			160	mV
I_d	Quiescent Current				8	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA to 1A			0.5	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA V_i = 14.5 to 30 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA T_j = -55 to 150 ^oC		-1		mV/^oC
e_N	Output Noise Voltage	B = 10Hz to 100KHz		75		μV
SVR	Supply Voltage Rejection	f = 120 Hz	53			dB
V_i	Operating Input Voltage	$I_o \leq$ 1.5 A	15			V
R_o	Output Resistance	f = 1KHz		18		mΩ
I_{sc}	Short Circuit Current	V_i = 27 V		500		mA
I_{scp}	Short Circuit Peack Current			3		A

ELECTRICAL CHARACTERISTICS FOR L78S15 (refer to the test circuits, T_j = 25 ^oC, V_i = 23V, I_o = 500 mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage		14.4	15	15.6	V
V_o	Output Voltage	I_o = 1 A V_i = 17.5 V	14.25	15	15.75	V
ΔV_o	Line Regulation	V_i = 17.5 to 30 V V_i = 20 to 26 V			300 150	mV mV
ΔV_o	Load Regulation	I_o = 20 mA to 2 A			180	mV
I_d	Quiescent Current				8	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA to 1A			0.5	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA V_i = 17.5 to 30 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA T_j = -55 to 150 ^oC		-1		mV/^oC
e_N	Output Noise Voltage	B = 10Hz to 100KHz		90		μV
SVR	Supply Voltage Rejection	f = 120 Hz	52			dB
V_i	Operating Input Voltage	$I_o \leq$ 1.5 A	18			V
R_o	Output Resistance	f = 1KHz		19		mΩ
I_{sc}	Short Circuit Current	V_i = 27 V		500		mA
I_{scp}	Short Circuit Peack Current			3		A

ELECTRICAL CHARACTERISTICS FOR L78S18 (refer to the test circuits, T_j = 25 ^oC, V_i = 26V, I_o = 500 mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage		17.1	18	18.9	V
V_o	Output Voltage	I_o = 1 A V_i = 20.5 V	17	18	19	V
ΔV_o	Line Regulation	V_i = 20.5 to 30 V V_i = 22 to 28 V			360 180	mV mV
ΔV_o	Load Regulation	I_o = 20 mA to 2 A			200	mV
I_d	Quiescent Current				8	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA to 1A			0.5	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA V_i = 22 to 33 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA T_j = -55 to 150 ^oC		-1		mV/^oC
e_N	Output Noise Voltage	B = 10Hz to 100KHz		110		µV
SVR	Supply Voltage Rejection	f = 120 Hz	49			dB
V_i	Operating Input Voltage	$I_o \leq$ 1.5 A	21			V
R_o	Output Resistance	f = 1KHz		22		mΩ
I_{sc}	Short Circuit Current	V_i = 27 V		500		mA
I_{scp}	Short Circuit Peack Current			3		A

ELECTRICAL CHARACTERISTICS FOR L78S24 (refer to the test circuits, T_j = 25 ^oC, V_i = 33V, I_o = 500 mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage		23	24	25	V
V_o	Output Voltage	I_o = 1 A V_i = 27 V	22.8	24	25.2	V
ΔV_o	Line Regulation	V_i = 27 to 38 V V_i = 30 to 36 V			480 240	mV mV
ΔV_o	Load Regulation	I_o = 20 mA to 2 A			250	mV
I_d	Quiescent Current				8	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA to 1A			0.5	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA V_i = 8 to 25 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA T_j = -55 to 150 ^oC		-1.5		mV/^oC
e_N	Output Noise Voltage	B = 10Hz to 100KHz		170		µV
SVR	Supply Voltage Rejection	f = 120 Hz	48			dB
V_i	Operating Input Voltage	$I_o \leq$ 1.5 A	27			V
R_o	Output Resistance	f = 1KHz		23		mΩ
I_{sc}	Short Circuit Current	V_i = 27 V		500		mA
I_{scp}	Short Circuit Peack Current			3		A

ELECTRICAL CHARACTERISTICS FOR L78S05C (refer to the test circuits, T_j = 25 ^oC, V_i = 10V, I_o = 500 mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage		4.8	5	5.2	V
V_o	Output Voltage	I_o = 1 A V_i = 7 V	4.75	5	5.25	V
ΔV_o	Line Regulation	V_i = 7 to 25 V V_i = 8 to 12 V			100 50	mV mV
ΔV_o	Load Regulation	I_o = 20 mA to 1.5 A I_o = 2 A		 80	100	mV
I_d	Quiescent Current				8	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA to 1A			0.5	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA V_i = 7 to 25 V			1.3	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA T_j = 0 to 70 ^oC		-1.1		mV/^oC
e_N	Output Noise Voltage	B = 10Hz to 100KHz		40		µV
SVR	Supply Voltage Rejection	f = 120 Hz	54			dB
V_i	Operating Input Voltage	$I_o \leq 1.5$ A	8			V
R_o	Output Resistance	f = 1KHz		17		mΩ
I_{sc}	Short Circuit Current	V_i = 27 V		500		mA
I_{scp}	Short Circuit Peack Current			3		A

ELECTRICAL CHARACTERISTICS FOR L78S75C (refer to the test circuits, T_j = 25 ^oC, V_i = 12.5V, I_o = 500 mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage		7.15	7.5	7.9	V
V_o	Output Voltage	I_o = 1 A V_i = 9.5 V	7.1	7.5	7.95	V
ΔV_o	Line Regulation	V_i = 9.5 to 25 V V_i = 10.5 to 20 V			120 60	mV mV
ΔV_o	Load Regulation	I_o = 20 mA to 1.5 A I_o = 2 A		 100	140	mV
I_d	Quiescent Current				8	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA to 1A			0.5	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA V_i = 9.5 to 25 V			1.3	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA T_j = 0 to 70 ^oC		-0.8		mV/^oC
e_N	Output Noise Voltage	B = 10Hz to 100KHz		52		µV
SVR	Supply Voltage Rejection	f = 120 Hz	48			dB
V_i	Operating Input Voltage	$I_o \leq 1.5$ A	10.5			V
R_o	Output Resistance	f = 1KHz		16		mΩ
I_{sc}	Short Circuit Current	V_i = 27 V		500		mA
I_{scp}	Short Circuit Peack Current			3		A

ELECTRICAL CHARACTERISTICS FOR L78S09C (refer to the test circuits, T_j = 25 °C, V_i = 14V, I_o = 500 mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage		8.65	9	9.35	V
V_o	Output Voltage	I_o = 1 A V_i = 11 V	8.6	9	9.4	V
ΔV_o	Line Regulation	V_i = 11 to 25 V V_i = 11 to 20 V			130 65	mV mV
ΔV_o	Load Regulation	I_o = 20 mA to 1.5 A I_o = 2 A		 100	170	mV
I_d	Quiescent Current				8	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA to 1A			0.5	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA V_i = 11 to 25 V			1.3	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA T_j = 0 to 70 °C		-1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz		60		µV
SVR	Supply Voltage Rejection	f = 120 Hz	47			dB
V_i	Operating Input Voltage	$I_o \leq$ 1.5 A	12			V
R_o	Output Resistance	f = 1KHz		17		mΩ
I_{sc}	Short Circuit Current	V_i = 27 V		500		mA
I_{scp}	Short Circuit Peack Current			3		A

ELECTRICAL CHARACTERISTICS FOR L78S10C (refer to the test circuits, T_j = 25 °C, V_i = 15V, I_o = 500 mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage		9.5	10	10.5	V
V_o	Output Voltage	I_o = 1 A V_i = 12.5 V	9.4	10	10.6	V
ΔV_o	Line Regulation	V_i = 12.5 to 30 V V_i = 14 to 22 V			200 100	mV mV
ΔV_o	Load Regulation	I_o = 20 mA to 1.5 A I_o = 2 A		 150	240	mV
I_d	Quiescent Current				8	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA to 1A			0.5	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA V_i = 12.5 to 30 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA T_j = 0 to 70 °C		-1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz		65		µV
SVR	Supply Voltage Rejection	f = 120 Hz	47			dB
V_i	Operating Input Voltage	$I_o \leq$ 1.5 A	13			V
R_o	Output Resistance	f = 1KHz		17		mΩ
I_{sc}	Short Circuit Current	V_i = 27 V		500		mA
I_{scp}	Short Circuit Peack Current			3		A

ELECTRICAL CHARACTERISTICS FOR L78S12C (refer to the test circuits, T_j = 25 °C, V_i = 19V, I_o = 500 mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage		11.5	12	12.5	V
V_o	Output Voltage	I_o = 1 A V_i = 14.5 V	11.4	12	12.6	V
ΔV_o	Line Regulation	V_i = 14.5 to 30 V V_i = 16 to 22 V			240 120	mV mV
ΔV_o	Load Regulation	I_o = 20 mA to 1.5 A I_o = 2 A		 150	240	mV
I_d	Quiescent Current				8	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA to 1A			0.5	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA V_i = 14.5 to 30 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA T_j = 0 to 70 °C		-1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz		75		μV
SVR	Supply Voltage Rejection	f = 120 Hz	47			dB
V_i	Operating Input Voltage	$I_o \leq$ 1.5 A	15			V
R_o	Output Resistance	f = 1KHz		18		mΩ
I_{sc}	Short Circuit Current	V_i = 27 V		500		mA
I_{scp}	Short Circuit Peack Current			3		A

ELECTRICAL CHARACTERISTICS FOR L78S15C (refer to the test circuits, T_j = 25 °C, V_i = 23V, I_o = 500 mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage		14.4	15	15.6	V
V_o	Output Voltage	I_o = 1 A V_i = 17.5 V	14.25	15	15.75	V
ΔV_o	Line Regulation	V_i = 17.5 to 30 V V_i = 20 to 26 V			300 150	mV mV
ΔV_o	Load Regulation	I_o = 20 mA to 1.5 A I_o = 2 A		 150	300	mV
I_d	Quiescent Current				8	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA to 1A			0.5	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA V_i = 17.5 to 30 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA T_j = 0 to 70 °C		-1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz		90		μV
SVR	Supply Voltage Rejection	f = 120 Hz	46			dB
V_i	Operating Input Voltage	$I_o \leq$ 1.5 A	18			V
R_o	Output Resistance	f = 1KHz		19		mΩ
I_{sc}	Short Circuit Current	V_i = 27 V		500		mA
I_{scp}	Short Circuit Peack Current			3		A

ELECTRICAL CHARACTERISTICS FOR L78S18C (refer to the test circuits, T_j = 25 °C, V_i = 26V, I_o = 500 mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage		17.1	18	18.9	V
V_o	Output Voltage	I_o = 1 A V_i = 20.5 V	17	18	19	V
ΔV_o	Line Regulation	V_i = 20.5 to 30 V V_i = 22 to 28 V			360 180	mV mV
ΔV_o	Load Regulation	I_o = 20 mA to 1.5 A I_o = 2 A		 200	360	mV
I_d	Quiescent Current				8	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA to 1A			0.5	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA V_i = 20.5 to 30 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA T_j = 0 to 70 °C		-1		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz		110		μV
SVR	Supply Voltage Rejection	f = 120 Hz	43			dB
V_i	Operating Input Voltage	$I_o \leq$ 1.5 A	21			V
R_o	Output Resistance	f = 1KHz		22		mΩ
I_{sc}	Short Circuit Current	V_i = 27 V		500		mA
I_{scp}	Short Circuit Peack Current			3		A

ELECTRICAL CHARACTERISTICS FOR L78S24C (refer to the test circuits, T_j = 25 °C, V_i = 33V, I_o = 500 mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage		23	24	25	V
V_o	Output Voltage	I_o = 1 A V_i = 27 V	22.8	24	25.2	V
ΔV_o	Line Regulation	V_i = 27 to 38 V V_i = 30 to 36 V			480 240	mV mV
ΔV_o	Load Regulation	I_o = 20 mA to 1.5 A I_o = 2 A		 300	480	mV
I_d	Quiescent Current				8	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA to 1A			0.5	mA
ΔI_d	Quiescent Current Change	I_o = 20 mA V_i = 27 to 38 V			1	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA T_j = 0 to 70 °C		-1.5		mV/°C
e_N	Output Noise Voltage	B = 10Hz to 100KHz		170		μV
SVR	Supply Voltage Rejection	f = 120 Hz	42			dB
V_i	Operating Input Voltage	$I_o \leq$ 1.5 A	27			V
R_o	Output Resistance	f = 1KHz		28		mΩ
I_{sc}	Short Circuit Current	V_i = 27 V		500		mA
I_{scp}	Short Circuit Peack Current			3		A

Figure 4 : Dropout Voltage vs. Junction Temperature.

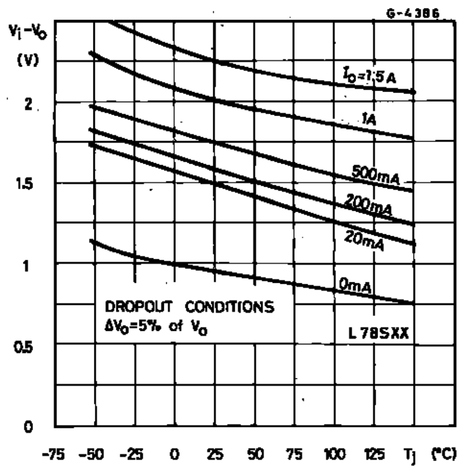


Figure 5 : Peak Output Current vs. Input/Output Differential Voltage.

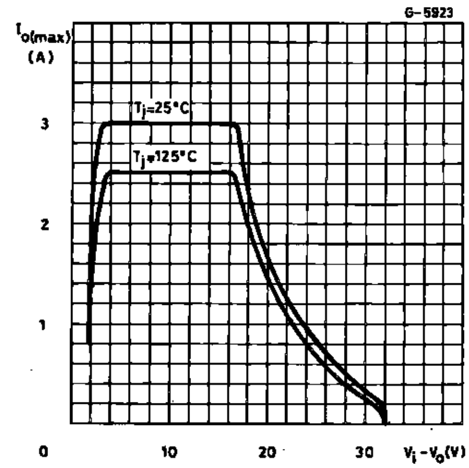


Figure 6 : Supply Voltage Rejection vs. Frequency.

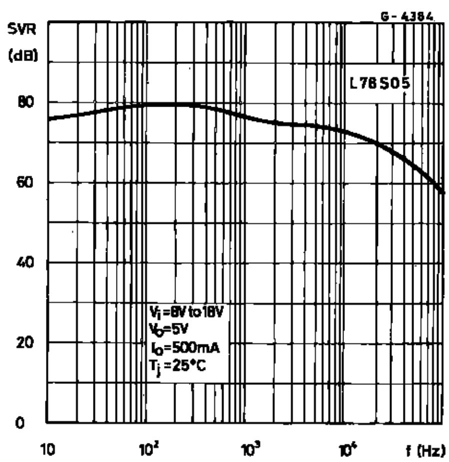


Figure 7 : Output Voltage vs. Junction Temperature.

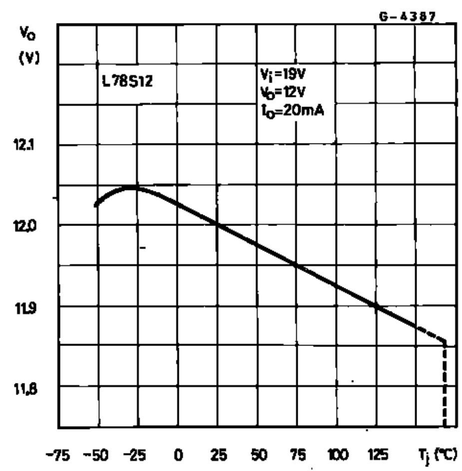


Figure 8 : Output Impedance vs. Frequency.

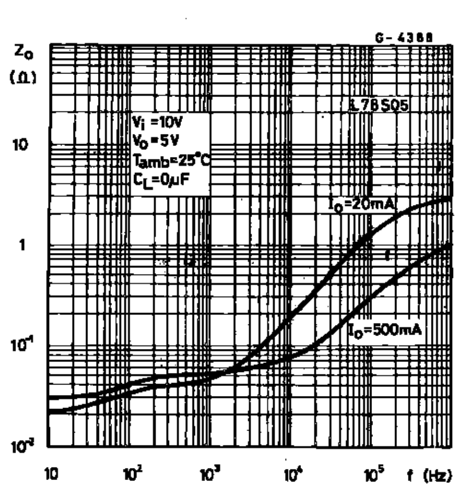


Figure 9 : Quiescent Current vs. Junction Temperature.

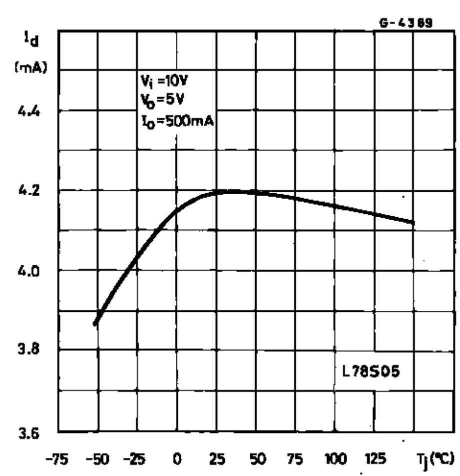


Figure 10 : Load Transient Response.

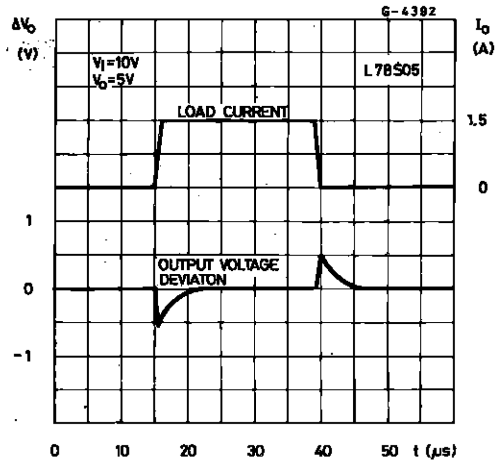


Figure 11 : Line Transient Response.

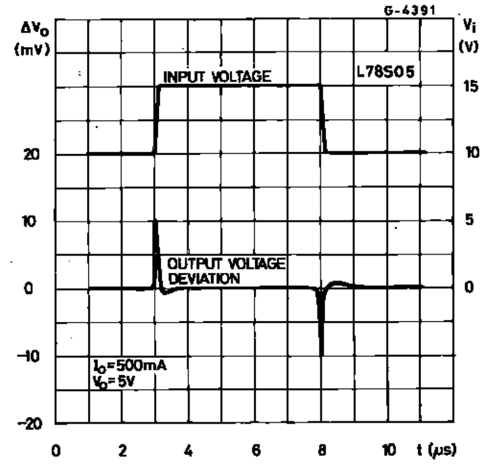


Figure 12 : Quiescent Current vs. Input Voltage.

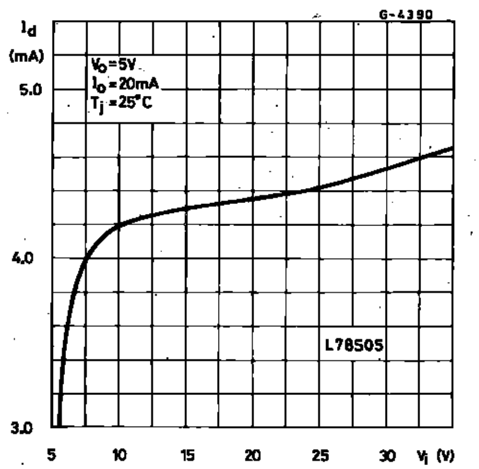
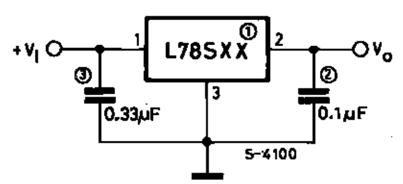
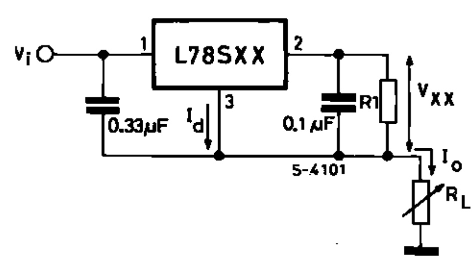


Figure 13 : Fixed Output Regulator.



Notes :
1. To specify an output voltage, substitute voltage value for "XX".
2. Although no output capacitor is needed for stability, it does improve transient response.
3. Required if regulator is located an appreciable dis-tance from power supply filter.

Figure 14 : Constant Current Regulator.



$$I_O = \frac{V_{XX}}{R_1} + I_d$$

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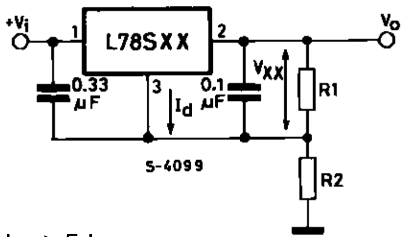
Figure 15 : Circuit for Increasing Output Voltage.



$I_{R1} \geq 5\ I_d$

$$V_0 = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + I_d R_2$$

Figure 16 : Adjustable Output Regulator (7 to 30V).

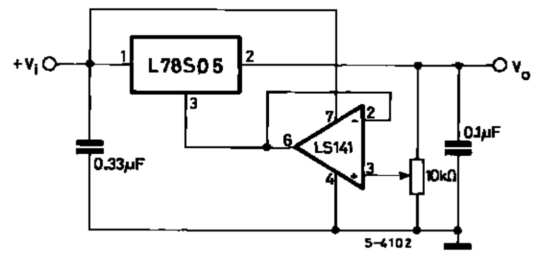
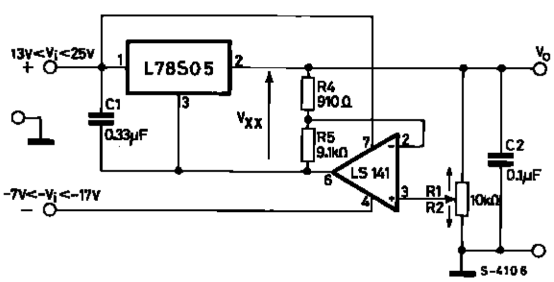
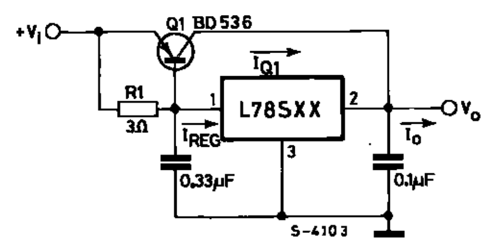


Figure 17 : 0.5 to 10V Regulator.



$$V_O = V_{XX}\ \frac{R_4}{R_1}$$

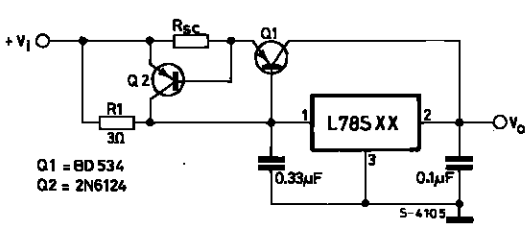
Figure 18 : High Current Voltage Regulator.



$$R_1 = \frac{V_{BEQ1}}{I_{REQ} - \dfrac{I_{Q1}}{\beta_{Q1}}}$$

$$I_O = I_{REG} + Q_1\left[I_{REG} - \frac{V_{BEQ1}}{R_1}\right]$$

Figure 19 : High Output Current with Short Circuit Protection.



$$R_{SC} = \frac{V_{BEQ2}}{I_{SC}}$$

Figure 20 : Tracking Voltage Regulator.

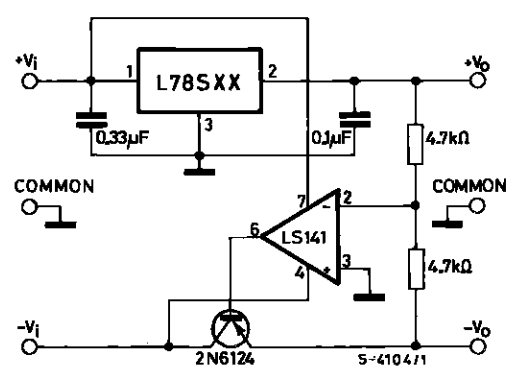
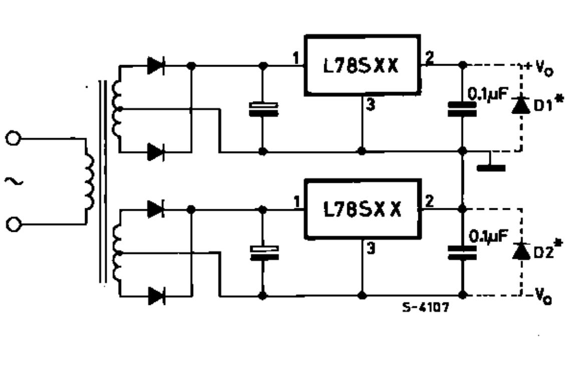


Figure 21 : Positive and Negative Regulator.



(*) D_1 and D_2 are necessary if the load is connected between + V_0 and – V_0.

Figure 22 : Negative Output Voltage Circuit.

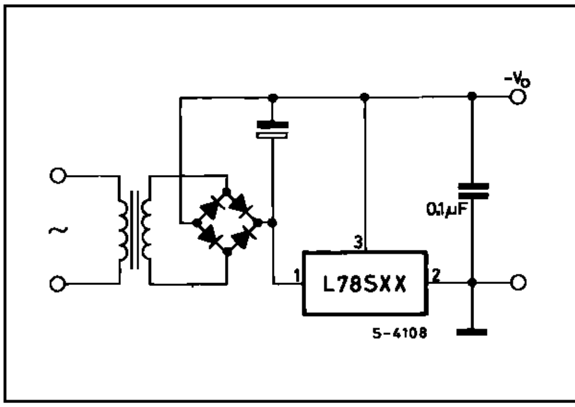


Figure 23 : Switching Regulator.

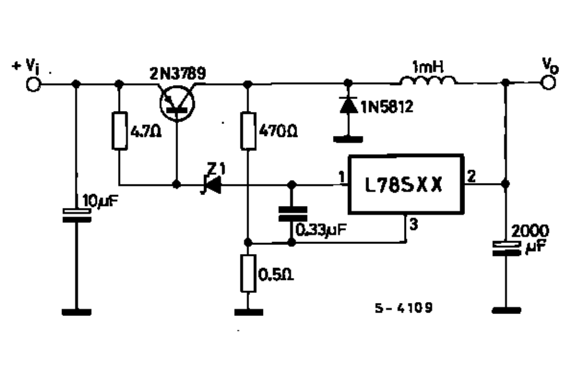
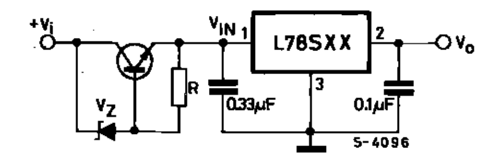
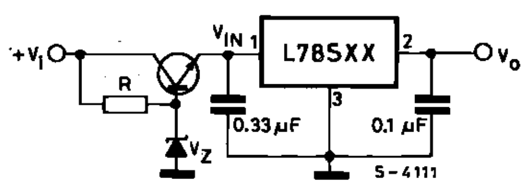


Figure 24 : High Input Voltage Circuit.



$V_{IN} = V_i - (V_Z + V_{BE})$

Figure 25 : High Input Voltage Circuit.



$V_{IN} = V_Z - V_{BE}$

Figure 26 : High Output VoltageRegulator.

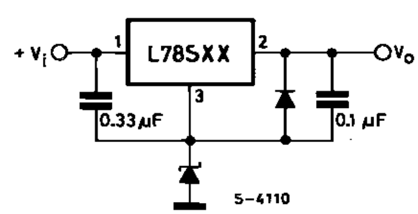
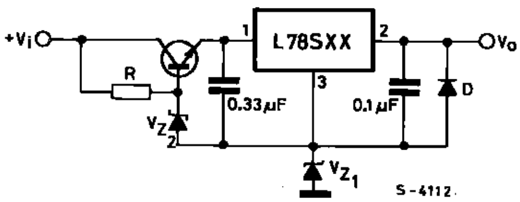
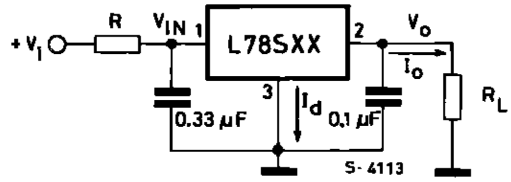


Figure 27 : High Input and Output Voltage.



$$V_O = V_{XX} + V_{Z1}$$

Figure 28 : Reducing Power Dissipation with Dropping Resistor.



$$R = \frac{V_{i(min)} - V_{XX} - V_{DROP(max)}}{I_{O(max)} + I_{d(max)}}$$

Figure 29 : Remote Shuntdown.

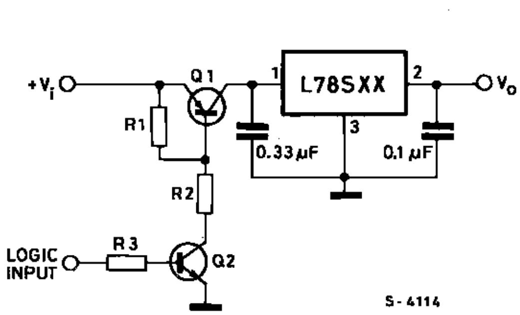
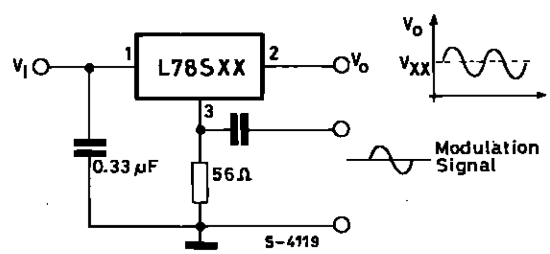
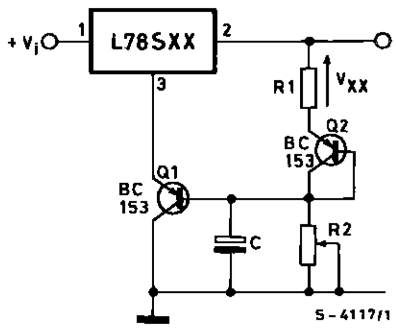


Figure 30 : Power AM Modulator (unity voltage gain, Io ≤ 1A).



Note : The circuit performs well up to 100KHz.

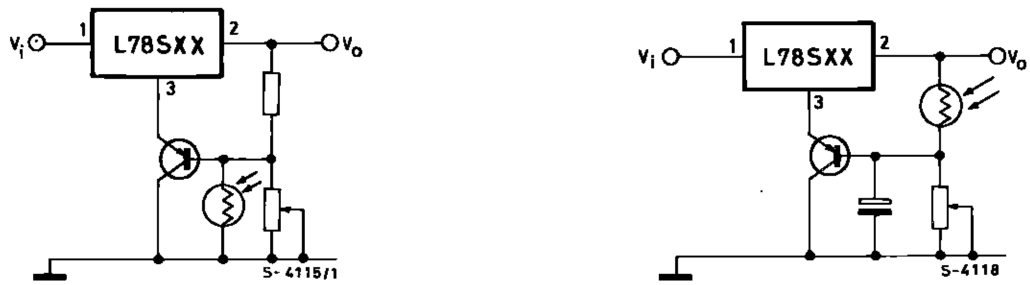
Figure 31 : Adjustable Output Voltage with Temperature Compensation.



$$V_O = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

Note : Q_2 is connected as a diode in order to compensate the variation of the Q_1 V_{BE} with the temperature. C allows a slow rise-time of the V_O

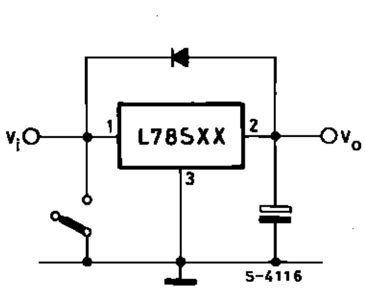
Figure 32 : Light Controllers ($V_{o\,min} = V_{xx} + V_{BE}$).



V_O falls when the light goes up

V_O rises when the light goes up

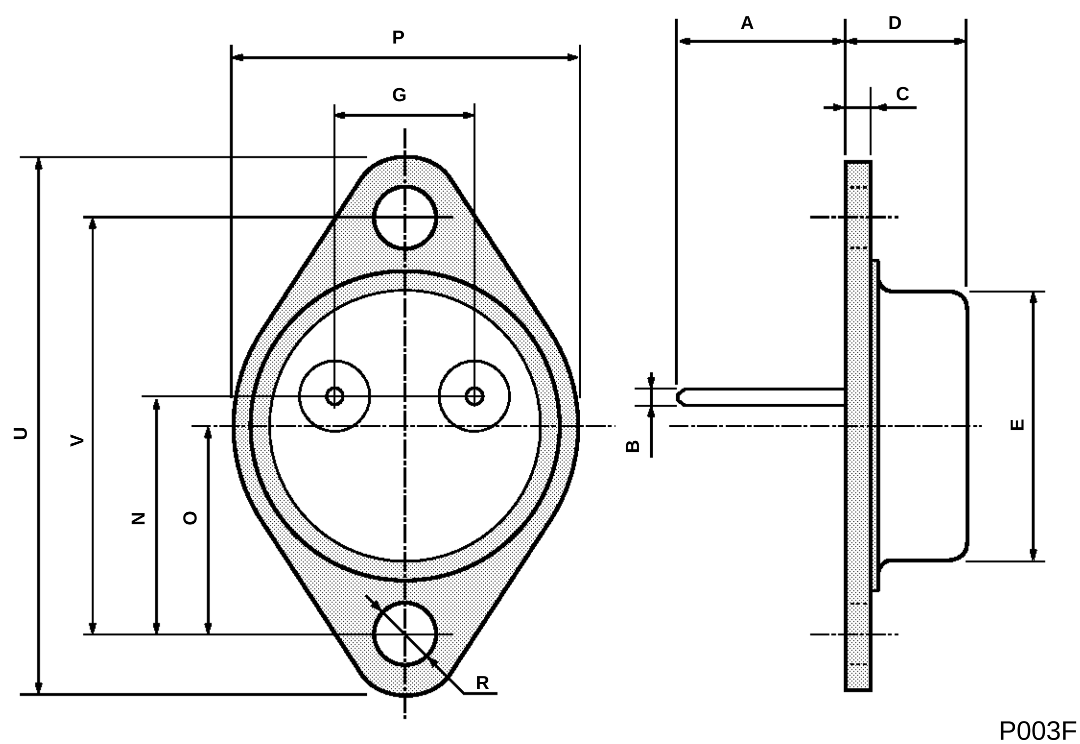
Figure 33 : Protection against Input Short-circuit with High Capacitance Loads.



Applications with high capacitance loads and an output voltage greater than 6 volts need an external diode (see fig. 33) to protect the device against input short circuit. In this case the input voltage falls rapidly while the output voltage decreases showly. The capacitance discharges by means of the Base-Emitter junction of the series pass transistor in the regulator. If the energy is sufficiently high, the transistor may be destroyed. The external diode bypasses the current from the IC to ground.

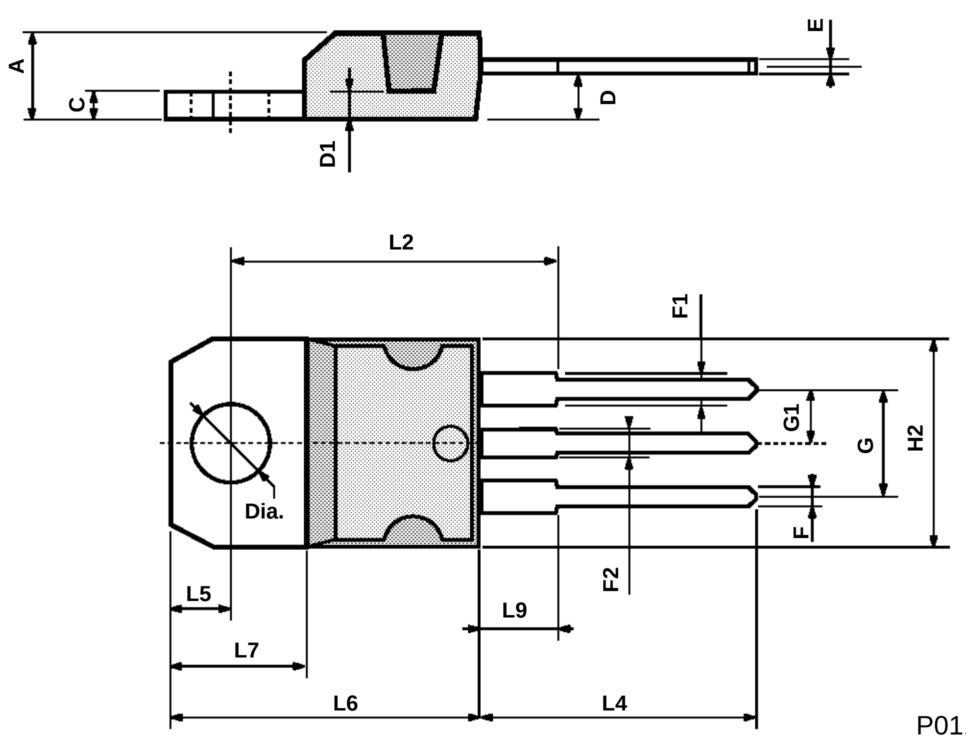
TO-3 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.00		13.10	0.433		0.516
B	0.97		1.15	0.038		0.045
C	1.50		1.65	0.059		0.065
D	8.32		8.92	0.327		0.351
E	19.00		20.00	0.748		0.787
G	10.70		11.10	0.421		0.437
N	16.50		17.20	0.649		0.677
P	25.00		26.00	0.984		1.023
R	4.00		4.09	0.157		0.161
U	38.50		39.30	1.515		1.547
V	30.00		30.30	1.187		1.193



TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.2		15.9	0.598		0.625
L7	6.2		6.6	0.244		0.260
L9	3.5		4.2	0.137		0.165
DIA.	3.75		3.85	0.147		0.151



P011C

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Příloha číslo 5

Katalogový list: Dioda BY359

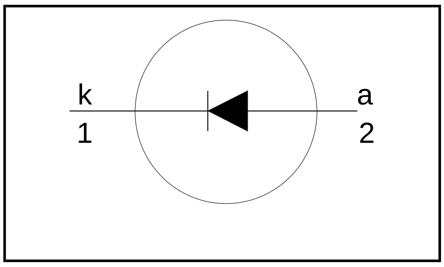
Damper diode fast, high-voltage

BY359-1500, BY359-1500S

FEATURES

- Low forward volt drop
- Fast switching
- Soft recovery characteristic
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_R = 1500 V

$V_F \leq$ 1.8 V / 2 V

$I_{F(RMS)}$ = 15.7 A

$I_{FSM} \leq$ 60 A

$t_{rr} \leq$ 600 ns / 350 ns

GENERAL DESCRIPTION

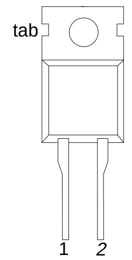
Glass-passivated double diffused rectifier diode featuring low forward voltage drop, fast reverse recovery and soft recovery characteristic. The device is intended for use in TV receivers and PC monitors.

The BY359 series is supplied in the conventional leaded SOD59 (TO220AC) package.

PINNING

PIN	DESCRIPTION
1	cathode
2	anode
tab	cathode

SOD59 (TO220AC)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{RSM}	Peak non-repetitive reverse voltage			-	1500	V
V_{RRM}	Peak repetitive reverse voltage			-	1500	V
V_{RWM}	Crest working reverse voltage			-	1300	V
$I_{F(peak)}$	Peak forward current	16-32kHz TV	BY359-1500	-	10	A
		31-70kHz monitor	BY359-1500S	-	7	A
$I_{F(RMS)}$	RMS forward current			-	15.7	A
I_{FRM}	Peak repetitive forward current	sinusoidal; a = 1.57		-	60	A
I_{FSM}	Peak non-repetitive forward current	t = 10 ms		-	60	A
		t = 8.3 ms		-	66	A
		sinusoidal; T_j = 150 ˚C prior to surge; with reapplied $V_{RWM(max)}$				
T_{stg}	Storage temperature			-40	150	˚C
T_j	Operating junction temperature			-	150	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air.	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

			BY359-1500		BY359-1500S		
SYMBOL	**PARAMETER**	**CONDITIONS**	**TYP.**	**MAX.**	**TYP.**	**MAX.**	**UNIT**
V_F	Forward voltage	I_F = 20 A	1.3	1.8	1.5	2.0	V
		I_F = 10 A; T_j = 150˚C	1.00	1.5	1.25	1.75	V
I_R	Reverse current	V_R = 1300 V	10	100	10	100	µA
		V_R = 1300 V; T_j = 100 ˚C	50	300	100	600	µA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

			BY359-1500		BY359-1500S		
SYMBOL	**PARAMETER**	**CONDITIONS**	**TYP.**	**MAX.**	**TYP.**	**MAX.**	**UNIT**
t_{rr}	Reverse recovery time	I_F = 2 A; V_R ≥ 30 V;	0.47	0.60	0.28	0.35	µs
Q_s	Reverse recovery charge	$-dI_F/dt$ = 20 A/µs	1.6	2.0	0.70	0.95	µC
V_{fr}	Peak forward recovery voltage	I_F = 10 A; dI_F/dt = 30 A/µs	11.0	-	17.0	-	V

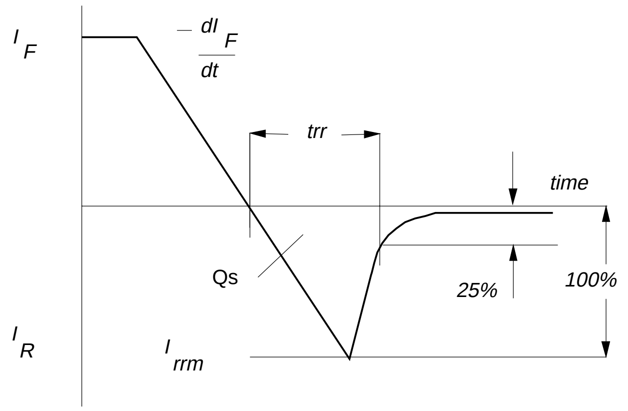


Fig.1. Definition of t_{rr}, Q_s and I_{rrm}

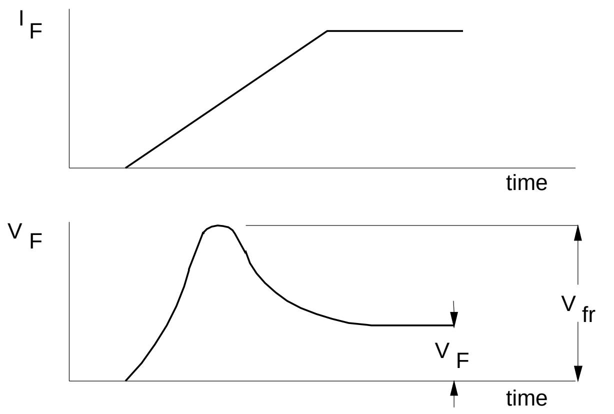


Fig.2. Definition of V_{fr}

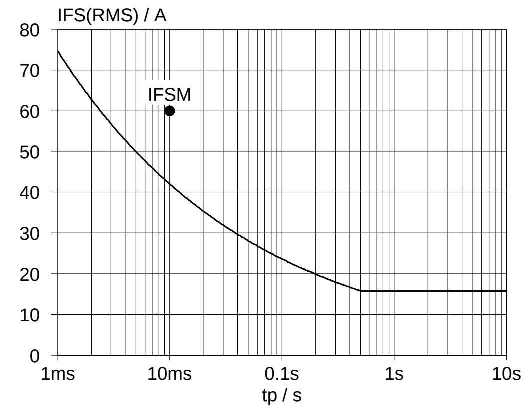


Fig.3. Maximum non-repetitive rms forward current. $I_F = f(t_p)$; sinusoidal current waveform; T_j = 150˚C prior to surge with reapplied V_{RWM}.

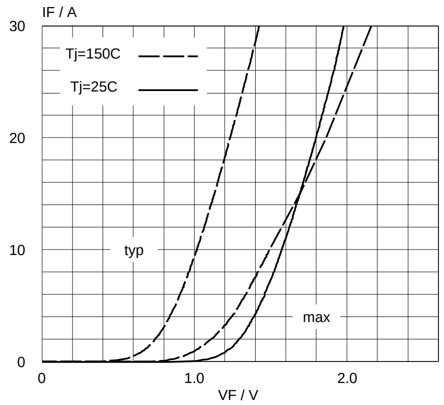


Fig.5. BY359-1500 forward characteristic $I_F = f(V_F)$; parameter T_j

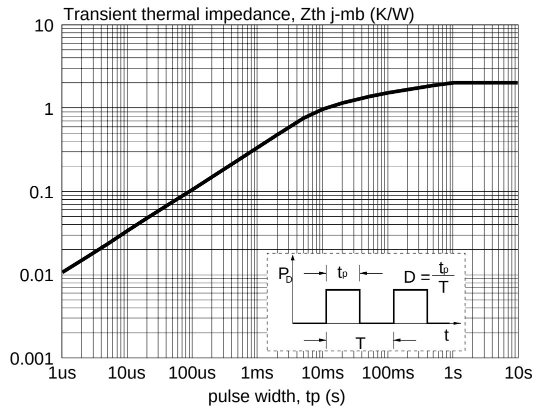


Fig.4. Transient thermal impedance $Z_{th} = f(t_p)$

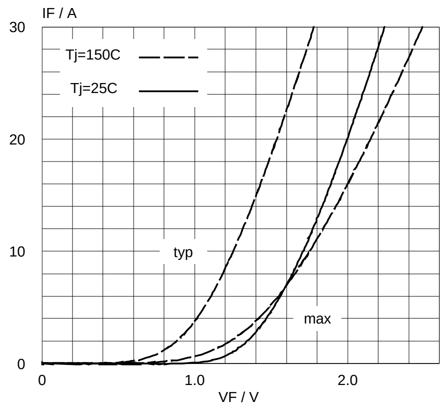


Fig.6. BY359-1500S forward characteristic $I_F = f(V_F)$; parameter T_j

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

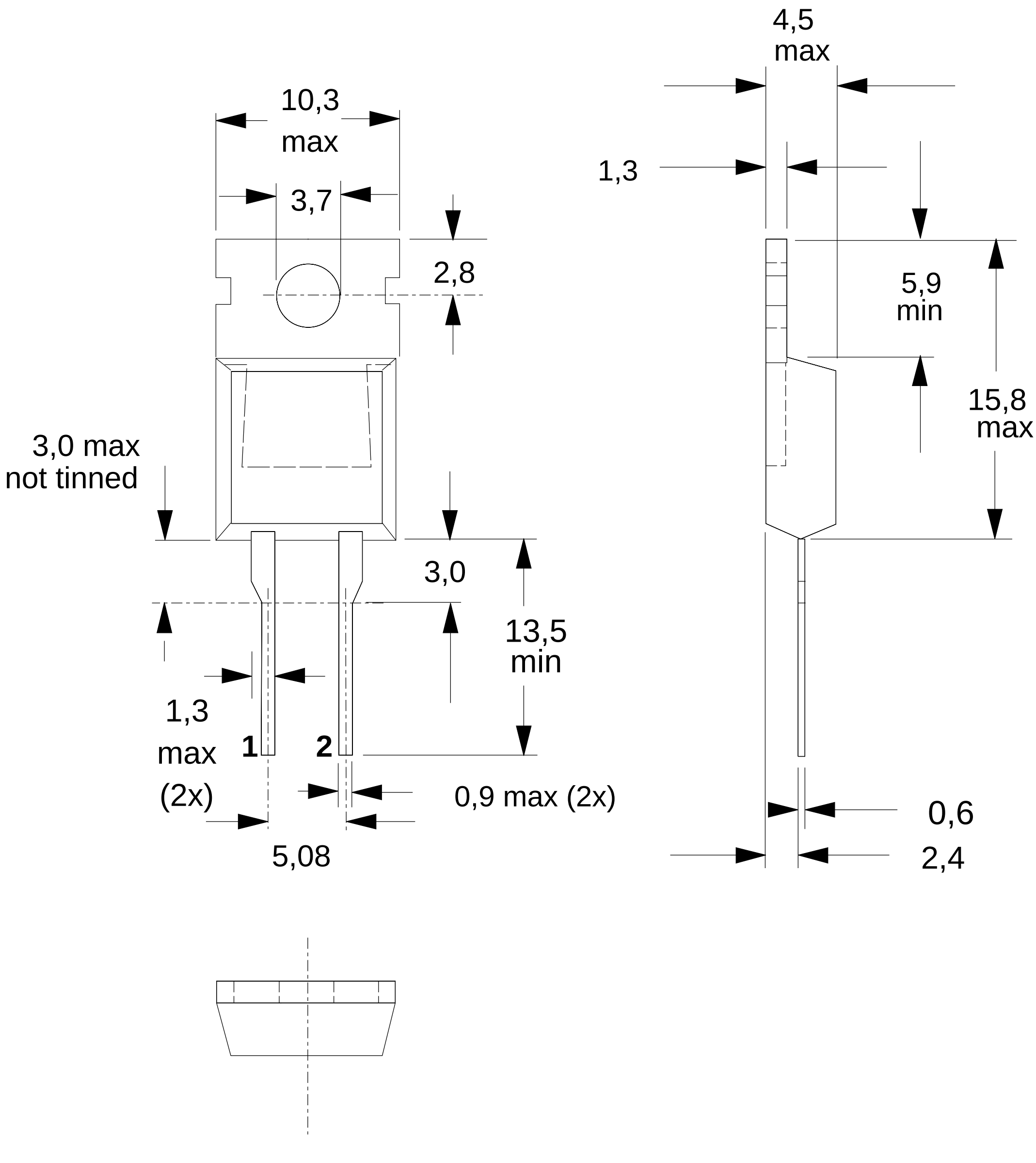


Fig.7. SOD59 (TO220AC). pin 1 connected to mounting base.

Notes
1. Refer to mounting instructions for TO220 envelopes.
2. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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