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Second supervisor review of Master Thesis

Title: Using ML to Model and Optimize Chip Geometry for Improved Lithography
Author: Junaid Ahmad
Opponent: Prof. Dr. Georg Pelz

The goal of this thesis was to investigate the impact of chip geometries on IC manufacturability in terms of number of chips on a wafer and reticle utilization. So far, the creation of an IC's layout comprised major parts of manual work and easily took weeks or even months for a single layout. With the advent of layout synthesis this can be largely automated, which especially holds for discrete devices, e.g. MOSFETs. As meanwhile also the electrical or thermal performance of discrete devices can be automatically simulated via finite element simulation, the optimization of these devices can be extended from

- Manually optimizing the layout to meet all performance requirements, while minimizing chip area

to

- Automatically optimizing the layout to meet all performance requirements, while obtaining
  - the maximum number of chips from a wafer and
  - the maximum reticle utilization, thus improving lithography-throughput

While the ML-based predictors for device performance were already available, Mr. Ahmad created ML-based predictors, mapping the chip's length and width onto the number of chips on a wafer and the reticle utilization. With this, he could optimize the

chip layout according to the second bullet point above. This was done based on an existing implementation of Differential Evolution. With his work, Mr. Ahmad has created a proof of concept for future improvements in IC development.

The work was carried out in reasonable and largely independent fashion. The thesis is well written, but comprises some smaller imprecisions. All in all, I recommend awarding the thesis the grade **1,3 (sehr gut)**.

Munich, 17.8.2023

Prof. Dr. Georg Pelz